APPLICATION NOTES

INTRODUCTION

The MECL family of monolithic integrated circuits consists of a wide selection of emitter coupled current mode logic circuits. Since MECL employs transistors in the non-saturating mode, it is inherently the fastest type of logic available. MECL is produced in two temperature ranges: the MC300 Series (-55°C to +125°C) and the MC350 Series (0°C to +75°C). Supply voltage is nominally -5.2 V ± 10% which yields a power dissipation between 35 and 40 mW per gate. Delay times range from 5 ns to 10 ns. The noise margin for all possible noise inputs is 200 mV or better over the full temperature range for at least 90% of the devices tested at a fan-out of one. Noise margin at room temperature is typically 300 mV.

The MECL gate employs a differential amplifier input, resulting in high input impedance, and good rejection of power supply variations. The very low output impedance of the emitter followers results in high fan-out and fast risetime for capacitive loads. Resistors and logic levels are chosen to prevent saturation of the input transistors, thus eliminating storage time. The 1.24 k resistor as shown in Figure 1 stabilizes circuit operation for wide variations of transistor β. A logical "1" for MECL is -.75 V which corresponds to one base-emitter voltage drop below ground. Logical "0" is -1.55 V which yields a nominal voltage swing of 800 mV.

Normal circuit operations is as follows: a fixed reference voltage of -1.15 V is applied to the V_{BB} input as shown in Figure 1. This voltage is chosen half way between the "0" and "1" logic levels which establishes the noise margins of the basic circuit. For example with no input to the gate, A_1, A_2 at a zero level or less, transistors A_1 and A_2 will be in a cutoff condition. Point E will now be one V_{B-E} drop below V_{BB} or at -1.90 V. For a logic "0" input A_1 and A_2 are forward biased by only .35 V which is insufficient to cause any current flow. If a logic "1" is now applied to A_1 or A_2, point E is one V_{B-E} drop lower in potential or (-.75 V) -.75 V or -1.50 V. Transistor B is now only forward biased by .35 V which leaves it cutoff. The current that passed through B has now been switched to the input transistor. The current through B was $\frac{-1.90\text{ V} - (-5.2\text{ V})}{1.24\text{ k}} = 2.66$ mA while the current for a "1" input is $\frac{-1.50\text{ V} - (-5.2\text{ V})}{1.24\text{ k}} =$ 2.98 mA which yields a gate that draws almost constant current.

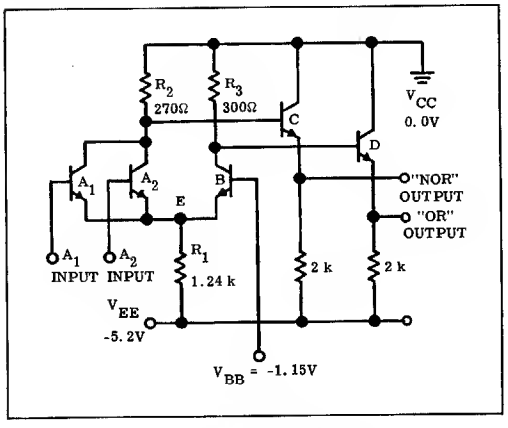


FIGURE 1 — OPERATION OF THE BASIC MECL GATE

The voltage at the collector of B (when conducting) is 0 - (300Ω x 2.66 mA) = -800 mV, while the voltage across the 270Ω resistor for a "1" input is 0 - (270Ω x 2.98 mA) = 800 mV. Transistors C and D are emitter followers; therefore the "NOR" and "OR" output voltage will follow the respective base voltage with a difference of -.75 V. If inputs are all low (logic "0"), the base of C will be at ground potential and the NOR output will be -.75 V (logic "1"). If one or more of the inputs are high, the base of C is at -.800 V and the NOR output drops to a logic "0". Operation of the OR output is similar only with no logic inversion.

The ratios of the collector resistors to the emitter resistor of the differential inputs determine the output "0" levels. Since accurate ratios of resistors are easier to obtain than absolute values of resistance, MECL output levels exhibit good uniformity from device to device. The absolute values of resistance are chosen as a compromise between speed of operation and power dissipation. As the power supply voltage is increased, the "0" level will move more negative while the "1" level remains constant. If V_{BB} is obtained from a Bias Driver connected to the same supply, the reference voltage will track with supply voltage changes or temperature variations, thus keeping V_{BB} in the center of the logic levels. At V_{EE} = -6 V for example, the nominal logic swing is 1.0 V. Not only is the logic swing increased and the noise margin bettered by about 50 mV, but power dissipation is increased as the square of the voltage. It is seen that the choice of V_{EE} = -5.2 V is a compromise between noise immunity and power dissipation. Nominal power dissipation for the basic gate is 37 mW while worst case should be considered as 20% higher.

Since the "1" level output is clamped to one V_{B-E} drop below V_{CC}, any noise appearing on the V_{CC} bus will appear on the output with very little attenuation. While any noise on the V_{EE} line will be attenuated by a factor of 4 to 5 which is primarily due to the ratio of R_1 to R_2 or R_1 to R_3. In most systems the ground plane or bus is the lowest impedance and therefore has the most constant potential and least induced noise. For this reason, the V_{CC} supply for MECL is usually obtained from ground. Another advantage of having V_{CC} at ground potential is that the gate outputs may be shorted to ground without drawing excessive current. If an output is accidently shorted to V_{EE} set at -5.2 V, the gate will draw excessive current (about 200 mA) but permanent damage does not occur until V_{EE} is increased to -8 V or -9 V and the current exceeds 400 mA.

Figure 2 shows the typical input characteristics of a MECL gate (input current vs. input voltage). Figure 3 shows output voltage vs output current over the full temperature range.

The input current is less than .1 mA and the output voltage level does not degrade for a load of 2.5 mA. D.C. fan-out is then 2.5 mA/.1 mA or 25. This is a D.C. fan-out and does not hold for high frequency operation. In fact, a maximum A.C. fan-out of 15 is recommended for high-speed operation. This decrease in fan-out is caused by the input capacitance of a gate, about 5 pF, and the wiring capacitance associated with a practical circuit. For a fan-out of 15, rise time is increased by about 5 ns while fall time will be increased by about 15 ns compared to the nominal values at a fan-out of one. The reason for the increase is that when switching from a zero to a one level, the low output impedance of the emitter follower charges the shunt capacitance, while switching from a one to a zero it is primarily the 2 k resistor that discharges the capacitance to the zero level.

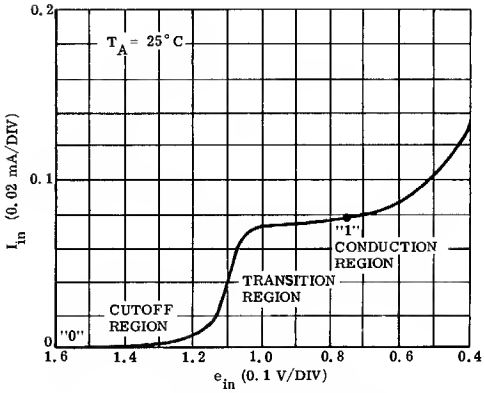


FIGURE 2 — INPUT CHARACTERISTICS OF A MECL GATE

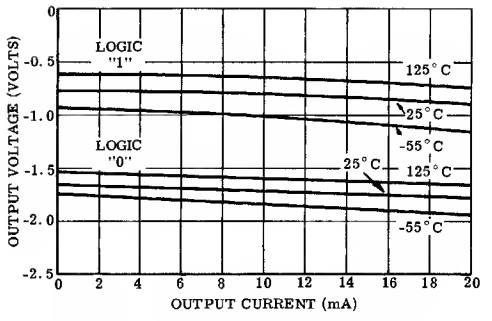


FIGURE 3 — OUTPUT VOLTAGE versus OUTPUT CURRENT

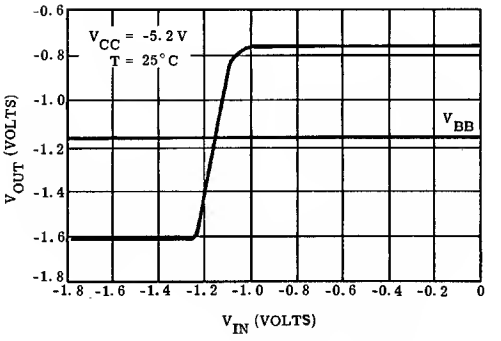


FIGURE 4 — TYPICAL "OR" TRANSFER CHARACTERISTICS

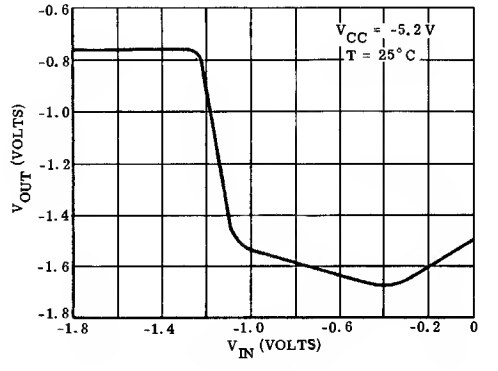


FIGURE 5 — TYPICAL "NOR" TRANSFER CHARACTERISTICS

The output of two gates may be connected in a "wired-OR" configuration, i.e. the gate outputs are wired together and whenever one or the other or both go high, the output goes high. For wired-OR operation, the worst case fan-out is 5 gate loads. Note that the pull down resistor is now effectively 1 k instead of 2 k and the fall time will be corresponding shorter.

Examination of the "OR" characteristic (Figure 4) shows that as the input voltage goes positive from a "0" level, the OR output may start to go positive at about -1.3 volts and will have reached a "1" level by about -1.0 V input. It may be shown that the 10%- to 90% transistion width is approximately 115 mV at 25°C regardless of circuit characteristics.* From Figure 1 it can be seen that as the input goes more positive, transistor B remains cut off and the output level remains constant. The "NOR" characteristics show that the width of the active region is about 200 mV. As the input goes more positive than the transition, the output continues to go more negative with a slope of about 1:4. This slope is due to the collector of the particular input transistor going more negative as the input goes more positive (the transistor is approaching saturation). As the input voltage approaches about -.4 volts at 25°C or -.6 V at 125°C, the input transistor reaches saturation. Saturation occurrs with about .45 volts forward bias on the base-collector junction at 25°C and about; .3 V forward bias at +125°C. Under saturation, the collector voltage will start to follow the base input and hence the output will also start to follow the input. The slope is about 0.8:1 since the voltage across the base to collector junction increases with heavier saturation. It should be noted that saturation does not start until an input of -.6 V is reached at 125°C ambient. The worst case "1" level is -.525 V which allows very slight saturation under absolute worst case conditions. The saturation is minimal so that the output rise and fall times are only slightly affected. For high speed operation, input levels should never go more positive than a most positive "1" level.

In consideration of maximum D.C. fan-out at maximum temperature, the input characteristics in Figure 2 show increasing current for -.6 to -.5 volts input, which may occur at worst case at high temperature. Fan-out does not actually decrease since if 25 inputs all drawing high current were connected to a gate with V_{out} = -.525 V, higher than normal current would be drawn from the emitter follower and drop the output level to perhaps -.58 V. The 25 loading gates now have a more negative input and will draw less current. These two effects balance each other and maximum fan-out need not be reduced at high temperature. Worst case fan-out cannot occur at high temperature for a most positive "1" level and actually increased fan-out is available.

The following curves illustrate worst case noise margins of MECL IC'S. The curves include the variations of

*Characterization of Integrated Logic Circuits, J.A. Narud and C.S. Meyer p 1551. Proceedings of the IEEE Special issue on Integrated Electronics, Dec. 1964

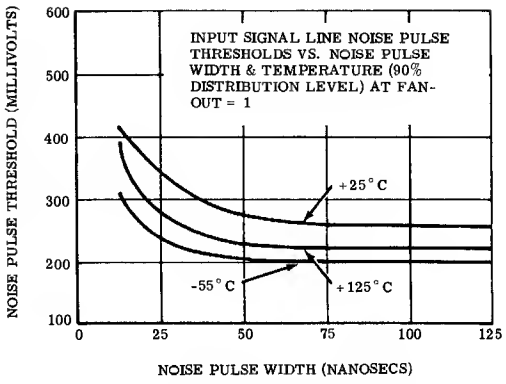


FIGURE 6 — INPUT SIGNAL LINE NOISE PULSE THRESHOLDS versus NOISE PULSE WIDTH AND TEMPERATURE

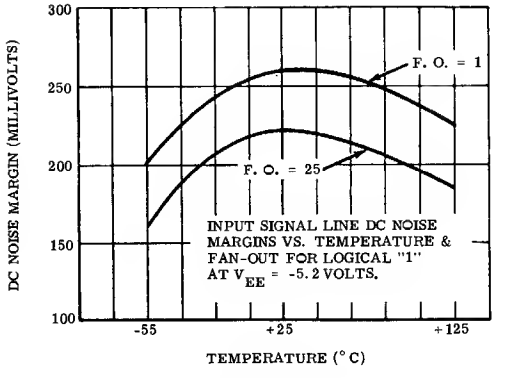


FIGURE 7 — INPUT SIGNAL LINE D.C. NOISE MARGIN versus TEMPERATURE AND FAN-OUT

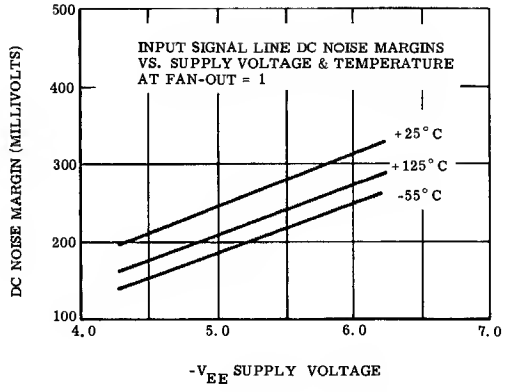


FIGURE 8 — INPUT SIGNAL LINE D.C. NOISE

V_{BB} and assure that 90% of the devices tested will have greater noise immunity than that shown:

Noise margins are slightly better for noise injected on the V_{CC} supply to the MECL gate under test and about four times better for noise injected on the V_{EE} supply.

Since the MECL gate has a differential amplifier input, it is of interest to note the common and differential mode gains. To measure these gains, one input transistor and the reference transistor are biased in the active region, i.e. neither transistor is cut off or saturated. To measure the common mode gain, a gate input such as (A_2) and the (V_{BB}) input are commoned. (Refer to Figure 1.) A nominal input of -1.15 V will center both transistors in the active region. An incremental voltage is now applied to the input while the "NOR" or "OR" output voltage with respect to common is recorded. The "NOR" common mode gain is approximately 1/9 or -19 dB while the "OR" common mode gain is about 1/7.5 or -17.5 dB. The difference arises due to the values of the collector resistors being different (270 and 300 ohms). The differential gain of the input is measured by connecting the V_{BB} input to -1.15 V and applying an incremental voltage centered around -1.15 V to an input transistor such as A_2, the "NOR" or "OR" output voltage is then noted with respect to ground. The differential "NOR" gain is about 5.6 or 14.5 dB while the differential "OR" gain is typically 6.0 application note AN-187. 100 foot twisted pair lines may be driven without problems by using MECL. The "OR" and "NOR" outputs of a gate drive one end of the line while a logic input and the V_{BB} input of a gate act as a differential receiver for the line. The line is terminated at the receiver input with a resistor of about 130Ω.

A better understanding of MECL may also be obtained from the typical curves (Figures 9, 10, and 11) that follow. These curves will answer system questions, concerning power dissipation vs temperature and supply voltage, and change in transfer characteristics with change in supply voltage.

GENERAL DESIGN RULES FOR MECL

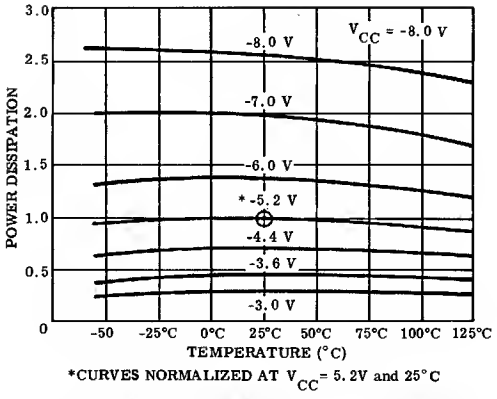
1. The maximum recommended A.C. fan-out for MECL is 15 unit input loads. D.C. fan-out is 25 unit loads. The A.C. fan-out is lower than the D.C. fan-out due to the increase in fall time and rise time with high fan-out. Also, if high fan-outs and long leads are used, overshoot due to lead inductance becomes a problem.

2. The Bias Driver (MC304, MC354) will fan-out to 25 gate loads. A dual gate or Half Adder is equivalent to two gate input loads for the Bias Driver.

3. Each $\overline{J}$ or $\overline{K}$ input to a flip flop is equivalent to one and one-half loads. For example, a $\overline{J}$ and $\overline{K}$ input tied together as a flip flop clock input would be a load of three, allowing a gate to drive five flip flops. All other inputs are a load of unity.

4. The outputs of two gates may be tied together to perform the "wired-OR" function, in which case a maximum fan-out of 5 is allowed. If only one pull down resistor is utilized, each additional common output is equivalent to one gate load. For example, if 6 gates are wired together with only one pull-down resistor connected, the fan-out would be (15) -5 or a fan-out of 10 remaining.

5. All unused inputs must be tied to V_{EE} for reliable operation. As seen from the gate input characteristics, the input impedance of a gate is very high when at a low level voltage. Any leakage to the input and/or wiring capacity of the gate will gradually build up a voltage on the input. This may ef-



*CURVES NORMALIZED AT V_{CC} = 5.2V and 25°C

FIGURE 9 — NORMALIZED POWER DISSIPATION FOR A MECL SYSTEM versus TEMPERATURE AND SUPPLY VOLTAGE

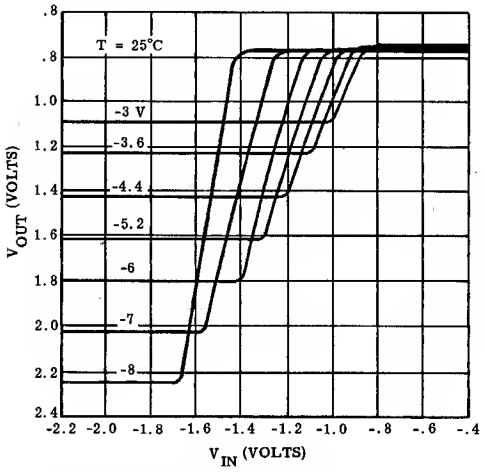


FIGURE 10 — TYPICAL "OR" TRANSFER CHARACTERISTICS versus SUPPLY VOLTAGE

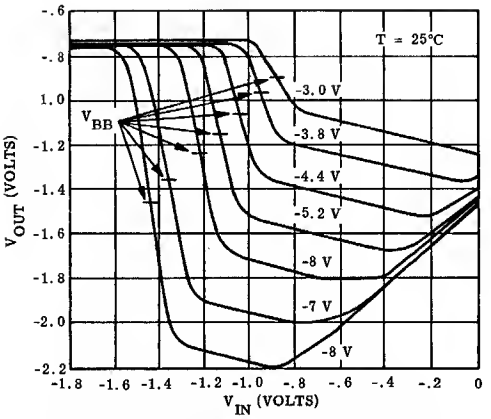


FIGURE 11 — TYPICAL "NOR" TRANSFER CHARACTERISTICS versus SUPPLY VOLTAGE

fect noise immunity of the gate or hinder switching characteristics at low repetition rates. Returning the unused inputs to V_{EE} insures no buildup of voltage on the input and a noise immunity dependent only upon the inputs used.

6. A recommended maximum of three input expanders should be used. For example, the MC306/MC307, MC356/MC357 gates would then have a fan-in of 18 available. If more than three input expanders are used, the NOR output rise and fall times suffer noticeably because of the increased capacitance at the collector node of the input transistors. For low frequencies, higher fan-ins may be employed if rise and fall times are of no significance.
7. Each gate package must have external bias supplied (V_{BB}) except for gates with internal reference such as MC312, MC313, MC362A, MC363, MC369, and the flip flops.

MECL IC's -55°C to +125°C

MC301	5-input OR, NOR
MC302	DC R-S Flip Flop, Outputs buffered, Reset input expandable
MC303	Half Adder--Sum, Carry, NOR
MC304	Bias Driver
MC305	5-input Expander
MC306	Expandable 3-input OR, NOR
MC307	Expandable 3-input OR, NOR, No pull-down resistors
MC308	J-K Flip Flop, DC R-S, Buffered outputs
MC309	Dual 2-input NOR, Both pull-down resistors
MC310	Dual 2-input NOR, One pull-down resistor, One optional
MC311	Dual 2-input NOR, One optional pull-down resistor
MC312	Dual 3-input NOR
MC312A	Dual 3-input NOR with Bias Driver
MC313F	Quad 2-input NOR with Bias Driver
MC314	J-K Flip Flop, DC R-S, High speed, Buffered outputs
MC315	Line Driver
MC316	Lamp Driver
MC317	Lever Translator MECL to DTL
MC318	Level Translator DTL to MECL

MECL IC's 0° to +75°C

MC351	5-input OR, NOR
MC352	DC R-S Flip Flop, No output buffers, Reset input expandable
MC352A	Same as MC302
MC353	Half Adder--Sum, Carry, NOR
MC354	Bias Driver
MC355	5-input Expander
MC356	Expandable 3-input OR, NOR
MC357	Expandable 3-input OR, NOR, No pull-down resistors
MC358A	J-K Flip Flop, DC R-S, Buffered outputs
MC359	Dual 2-input NOR, Both pull-down resistors
MC360	Dual 2-input NOR, One pull-down resistor, One optional
MC361	Dual 2-input NOR, One optional pull-down resistor
MC362	Dual 3-input NOR
MC362A	Dual 3-input NOR with Bias Driver
*MC363F	Quad 2-input NOR with Bias Driver
MC364	J-K Flip Flop, DC R-S, High speed, Buffered outputs
MC365	Line Driver
MC366	Lamp Driver
MC367	Level Translator MECL to DTL
MC368	Level Translator DTL to MECL
*MC369G	Dual-2 OR, NOR Clock Driver and High speed gate
*MC369F	Dual-4 OR, NOR Clock Driver and High speed gate

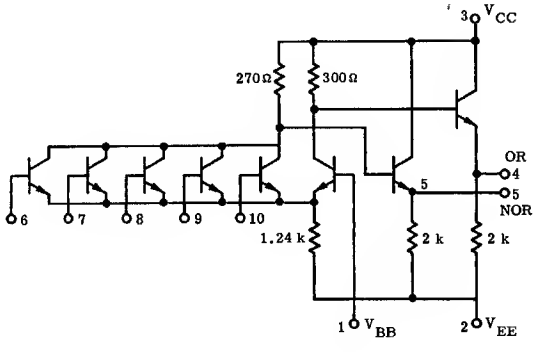
*F indicates a 14 lead flat package
*G indicates a TO-5 type package

TABLE 1 — MECL LOGIC ELEMENTS

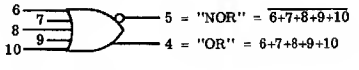
THE MECL FAMILY OF IC LOGIC ELEMENTS

The following section includes a complete explanation of each logic element. Schematics, logic diagrams, logic equations, and truth tables, where applicable, are included along with a detailed description of each circuit.

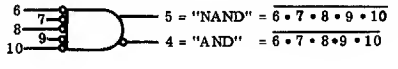
5 INPUT OR, NOR: MC301, MC351



POSITIVE LOGIC
SINGLE GATE

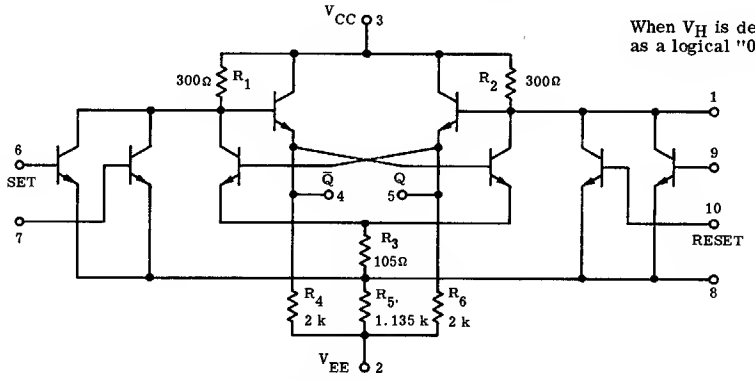


NEGATIVE LOGIC
SINGLE GATE

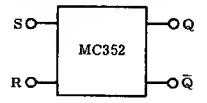


The 5-input gate obtains the maximum number of inputs for a standard TO-5 10-pin can. A pair of the gates may be wire-OR'd to form a 10-input gate. If desired, both NOR's and OR's may be wired together giving a gate that has the properties of a single gate with a fan-out of 5, fast fall time, and 10 inputs. Nominal power dissipation of the gate is 37 mW over the temperature range. Typical propagation delay is 8 ns with rise and fall times of 8 ns. As fan-out increases above 5, the fall time increases more rapidly than the rise time.

DC R-S FLIP-FLOP: MC352



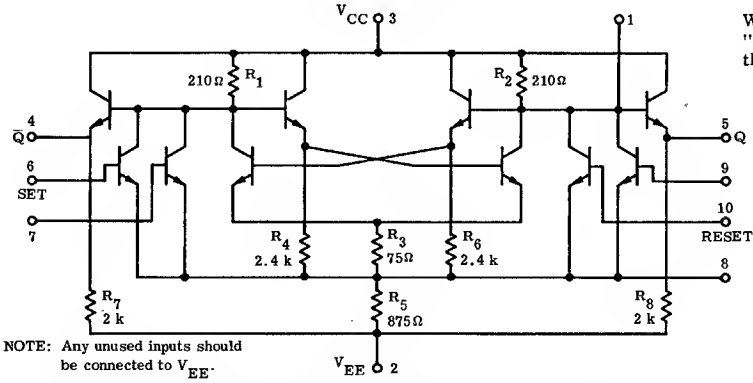
When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:



R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

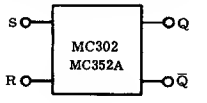
The D.C. R-S flip flop is most useful as a storage element. Dual inputs allow the OR function to be performed at the Set or Reset inputs. As may be noted from the schematic the Reset input is expandable. A maximum of 2 or 3 expanders is recommended for high speed operation since the additional collector node capacitance increases rise and fall times. The Set input may also be expanded by redefining inputs and switching the wiring of Q and $\bar{Q}$. The Set and Reset inputs should be standard MECL levels for optimun operation. Input rise and fall time is unimportant unless high speed operation is desired. Typically, the maximum speed of Set-Reset operation is 65 MHz, propagation delay 6.5 ns, rise and fall times 8 ns, and power dissipation 42 mW. The maximum Set-Reset speed is obtained for inputs with about 6 ns rise and fall times and a pulse widths of about 9 ns.

DC R-S FLIP-FLOP, OUTPUTS BUFFERED, RESET INPUT: MC302, MC352A



NOTE: Any unused inputs should be connected to V_{EE}.

When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:

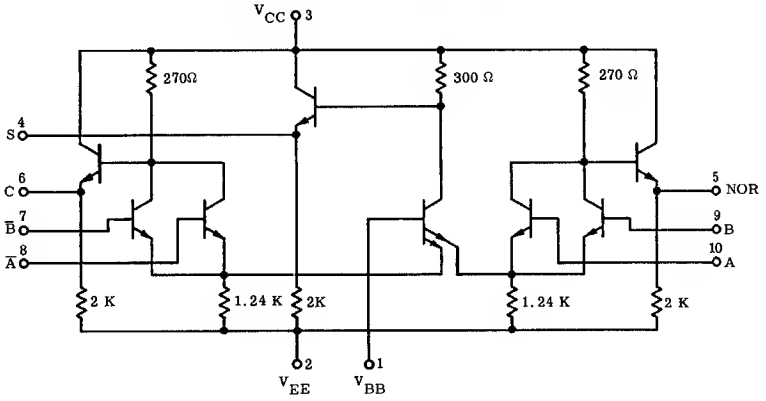


R	S	Q^{n+1}
0	1	1
1	0	0
0	0	Q^n
1	1	N.D.

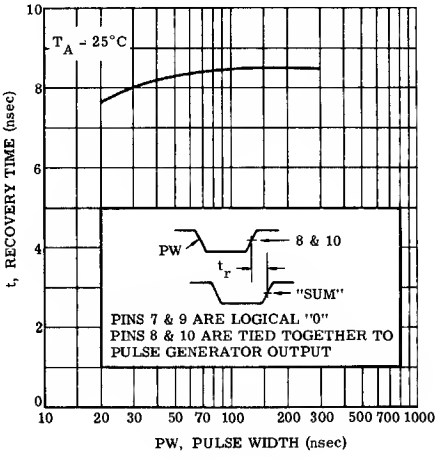
This flip flop is essentially the same as the MC352 with the exception that the outputs are isolated. The MC352 is sensitive to noise on the output lines because they feed back directly into the bases of the bistable transistors. The output emitter followers on the MC302, MC352A isolate each output from the respective base of each bistable transistor; giving about 800 mV noise margin for noise coupled into the output.

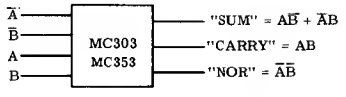
It should be noted that if both the set and reset inputs are high, both outputs will be low. Bringing both inputs to "0" simultaneously leaves the output in an undefined state, i.e. either a "0" or a "1". Typical parameters: rise time 11.5 ns fall time 12.5 ns, propagation delay time 11 ns, power dissipation 45 mW. The flip flop may be set and reset at a maximum rate of about 50 MHz. Optimum input pulses for 50 MHz operation should have rise and fall times of 6 ns or less with pulse widths of about 14 ns.

HALF ADDER, SUM, CARRY, NOR: MC303, MC353



RECOVERY CHARACTERISTICS WITH SIMULTANEOUS "0" ON ALL INPUTS





HALF ADDER Truth Table

Pin #	A 10	B 9	$\overline{A}$ 8	$\overline{B}$ 7	OUT 4
	Lo	Lo	Hi	Hi	Lo
	Lo	Hi	Hi	Lo	Hi
	Hi	Lo	Lo	Hi	Hi
	Hi	Hi	Lo	Lo	Lo

The Half Adder is a very useful element of the MECL family. It can be used as a digitally controlled inverter, a digital comparator, or to provide SUM, CARRY, and NOR, or SUM and $\overline{SUM}$ if desired. Normally two bits and their compliments are applied to the Half Adder so that two of the inputs are always high as shown in the schematic. If all four of the inputs are low, the V_{BB} transistor will be sinking twice the normal current at 25°C and the SUM output will drop to -2.3 V. This does no harm but to saturate the V_{BB} transistor. The graph shown above illustrates the recovery time at 25°C for saturation of the V_{BB} transistor. At higher temperatures it would take longer to recover.

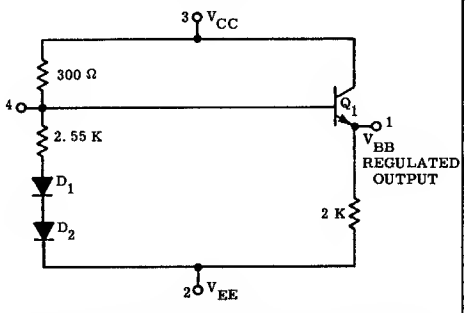
The Half Adder gating functions are the same as the general MECL gate shown in Figure 1 with the exception that the bias transistor performs the AND function, in that when both emitters are high, the SUM output is also high. With reference to the schematic and the letters representing the inputs, it is seen that the collector of the V_{BB} transistor is high when A and $\overline{B}$ are high or $\overline{A}$ and B are high. This represents the exclusive OR function or the sum of A and B. The Carry and NOR outputs may be wired together to form $A\overline{B} + \overline{A}B$ which may be recognized as $\overline{SUM}$. By the rules of Boolean Algebra: $SUM = A\overline{B} + \overline{A}B$ then $\overline{SUM} = \overline{A\overline{B} + \overline{A}B} = \overline{(A\overline{B})} \cdot \overline{(\overline{A}B)} = (\overline{A}+B)(A+\overline{B}) = \overline{A}\overline{B} + AB$ which is the wired output.

A digitally controlled inverter is one unique application of the MECL Half Adder. The inputs are connected in the same manner as for the SUM function. If A is considered as the digital information input and $\overline{B}$ as the control level (inversion or not inversion), then A appears at the S output if $\overline{B}$ is high and $\overline{A}$ appears at the S output if B is high. Thus A or $\overline{A}$ is obtained on the same wire according to the level of B.

The propagation delay of the circuit is typically 8 ns for the SUM output and 6 ns for the Carry and NOR outputs at room temperature at a fan-out of one gate. Rise times are typically 6.5 ns for all outputs while fall times are 8.5 ns for SUM and 8.0 ns for NOR and CARRY. Typical power dissipation is 65 mW.

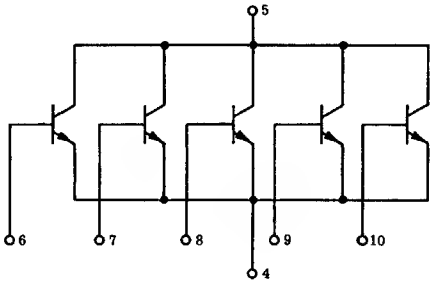
The Half Adder is shown in a digital comparator circuit and a five bit asynchronous adder in the last section of the paper.

BIAS ORIVER: MC304, MC354



The Bias Driver provides a temperature and voltage compensated reference for MECL logic. Any of the three MECL voltages may be grounded, but the common voltage of the Bias Driver must correspond to that of the logic system. The device has a unique application when coupling a signal through a capacitor to pin 4. First the gate acts as a level translator from any voltage to MECL levels. If the input is 800 mV p-p, the standard MECL levels will appear at pin 1. For low level A. C. and R. F. inputs, the output will be centered in the active region of a MECL gate which may then be used as an amplifier. A low quality, high bandwidth differential amplifier may be obtained by using two bias drivers, one connected to a normal gate input and the other connected to the V_{BB} input of a MECL gate. The "OR" and "NOR" outputs then provide a very low impedance differential output. The A. C. input impedance of the Bias Driver is 250Ω in parallel with about 5 pF which will terminate a low impedance line fairly well. If V_{CC} contains excessive noise the output on pin 1 may be filtered by connecting a capacitor between pin 4 and 2. Typical power dissipation is 17 mW. The Bias Driver will fan-out to 25 unit input loads.

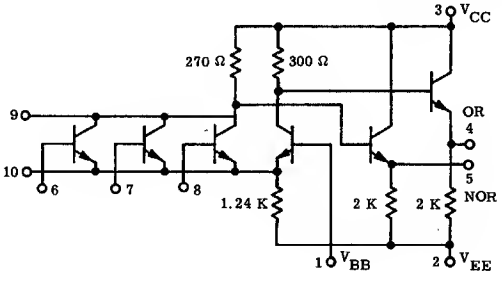
5 INPUT EXPANOER: MC305, MC355



The Gate Expander acts as a 5-input NOR gate when referring to the collectors or as a 5-input OR gate when referring to the emitters. This infers a resistor connected from the collector to a high level voltage while the emitter node is connected to a low voltage through another resistor.

The maximum number of recommended expanders to be used with a gate is three for high speed operation. If more than three expanders are used, the output rise and fall times will become excessive for high speed operation. When used with a MECL gate, power dissipation is negligible.

EXPANOABLE 3 INPUT OR, NOR: MC306, MC356

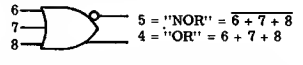


This gate may be expanded to 18 inputs by use of the MC305 or MC355, otherwise operation is the same as the basic MECL gate shown in Figure 1.

POSITIVE LOGIC

When V_H is defined as a logical "1" and V_L as a logical "0" the "OR"/"NOR" function is performed:

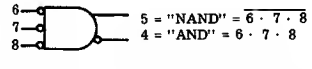
Single Gate



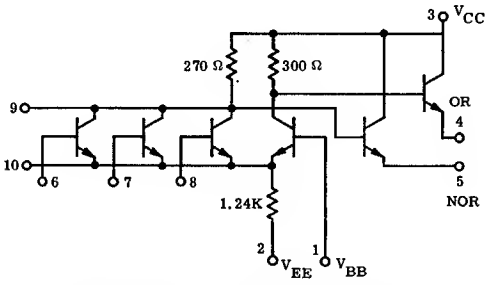
NEGATIVE LOGIC

Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "AND"/"NAND" function is performed:

Single Gate



Propagation delay time is typically 6.5 ns with a rise and fall time of 7 ns. Typical power dissipation is 37 mW.



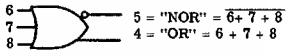
This gate is the same as MC306, MC356 except that the output pull-down resistors have been removed lowering the power dissipation. Propagation delay time is nominally 6.5 ns with rise and fall times of 7 ns with a normal load. The output of this gate may be wire-OR'd with other MC307, MC357 gates and one gate that has a pull-down resistor to -5.2 V. This will result in a large power savings since the gate only dissipates 16 mW at V_{EE} = -5.2 V. The maximum recommended number of gates connected in this manner is: 1 gate with a pull-down resistor, 14 gates with no pull-down resistor and the input of another MECL gate. In other words, the gate with the pull-down resistor, such as the MC301 or MC306, has a recommended maximum fan-out of 15. Each of the other wire-OR'd gates is the equivalent of one load, resulting in a fan-out of 1 to the input of another MECL gate.

EXPANDABLE 3 INPUT OR, NOR, NO PULL-DOWN RESISTORS: MC307, MC357

POSITIVE LOGIC

When V_H is defined as a logical "1" and V_L as a logical "0" the "OR"/"NOR" function is performed:

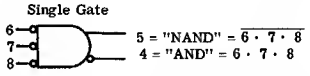
Single Gate



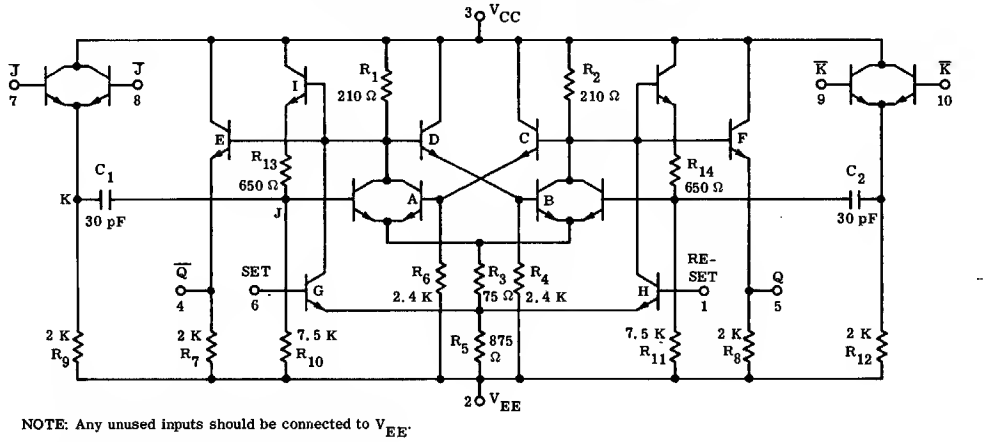
NEGATIVE LOGIC

Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "AND"/"NAND" function is performed:

Single Gate

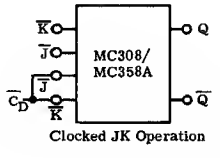


J-K FLIP-FLOP, DC R-S, BUFFERED OUTPUTS: MC308, MC358A



NOTE: Any unused inputs should be connected to V_{EE}.

When V_H is defined as a logical "1" and V_L as a logical "0", the function is as follows:



Clocked JK Operation

State#	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^{n+1}
1	ø	ø	0	Q^n
2	0	0	1	$\overline{Q}^n$
3	0	1	1	1
4	1	0	1	0
5	1	1	1	Q^n

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state.

Set-Reset operation is the same as MC302.

Operation of the MC308, MC358A

Transistors A and B form the "heart" or bistable pair of the flip flop. The collector of B is coupled back to the base of A through C, likewise D couples A back to B forming the bistable element. The output of A is buffered through E to give the $\overline{Q}$ output, while F buffers B to give the Q output. When the Set input (pin 6) goes to a high level (-0.75 V), the collector of G goes low pulling A and D low. The collector of B then goes high which holds the collector of A low through C. The flip flop is now Set to the "1" state, i.e. Q high and $\overline{Q}$ low. Likewise a high level in or a positive pulse on pin 1 resets the flip flop to the "0" state. Since the base of either A or B is at a one level (-0.75 V), the emitters will be one V_{BE} drop lower or at -1.50 V. The potential at the node between R_3 and R_5 is then -1.8 V which corresponds to a

continued

nominal 400 mV noise immunity for a Set or Reset input normally at -1.55 V (logic "0"). The Set, Reset input transistors may be considered to be in the active region at 0.65 V_{BE}.

The emitter of 1 also follows the collector of A and will yield standard MECL levels. The voltage at point J will then be approximately -1.1 or -1.85 due to the divider action of R_{13} and R_{10}. The $\overline{J}$ inputs on pins 7 and 8 act as emitter followers so that point K will be either -1.5 or -2.3 V. C_1 differentiates the input as it appears at point K. Whenever point K swings negative, nothing will happen, but when point K goes positive, a positive pulse will be coupled to the base of the transistor in parallel with A. If the collectors of the pair were high, they will be brought to a low level as if the flip flop had received a Set pulse. Likewise a positive going level at C_2 will reset the flip flop.

It should be noted that the input rise time must be less than a specified value to transfer enough charge through the capacitor to switch the flip flop. Also the maximum toggle speed of the flip flop is limited by the internal time constants associated with C_1 and C_2. If one of the $\overline{J}$ inputs is high it will inhibit a positive going level on the other $\overline{J}$ input and no pulse will be coupled into the flip flop, unless excessive amplitude, perhaps caused by ringing on the input line, is applied. If differences in the logic levels and ringing both add up to 250 mV for 10 ns or more, it is possible to trigger a flip flop falsely. For worst case design over temperature extremes overshoot should be a maximum of 100 mV. Note the discussion on overshoot for the MC369.

The classical J-K flip flop has its inputs labeled J, K, and C and operates on negative levels. The MECL $\overline{J}$-$\overline{K}$ flip flop is opposite, in that high levels inhibit and positive going clock transitions actually clock the flip flop. The MECL levels generally are preferrable since positive logic is more common than negative logic.

As may be seen from the truth table and the logic diagram for clocked $\overline{J}$-$\overline{K}$ operation, a dynamic "0" or negative going clock does not affect the flip flop when the other $\overline{J}$ and $\overline{K}$ inputs are at a static level. If $\overline{C_D}$ and $\overline{K}$ are low and $\overline{J}$ goes high, the flip flop will be set to a "1" on the Q output. Likewise if $\overline{C_D}$ and $\overline{J}$ are low while $\overline{K}$ goes high, the flip flop will be reset to zero. For normal clocked operation, $\overline{J}$ and $\overline{K}$ are static levels changed only when C_D is high (flip flop inhibited). The symbol in the truth table, ϕ, refers to a static level of either high or low. For state 1 in the truth table, the flip flop output, Q, will be the same level at time t = n + 1 as it was at t = n for a dynamic "0" transition of the clock between t = n and t = n + 1. For state 2 neither $\overline{J}$ or $\overline{K}$ are inhibited, and a dynamic clock will toggle the flip flop, i.e. at t = n + 1 the flip flop will be in the opposite state that it was in at t = n. For state 3, the $\overline{K}$ input is inhibited and a "1" will be shifted into the flip flop. Likewise a "0" will be shifted in for state 4. In state 5, both inputs are inhibited and the flip flop will not change state unless a Set or Reset input is received. Set - Reset inputs take priority over the $\overline{J}$-$\overline{K}$ inputs as may be seen from the schematic. If an uninhibited clock input is received while the Set or Reset level is true (high), a 20 ns pulse of about 400 mV level may appear on the output of the flip flop.

MC308, MC358A Characteristics

As in every $\overline{J}$ $\overline{K}$ flip flop the MC308, MC358A requires a minimum down time of the clock to ensure toggle. Minimum down time of the clock waveform is determined primarily by the discharge time constant of R_9 and C_1 which is nominally 60 ns. After a high level input appears at point K, at least 29 ns under worst case conditions must be allowed for the voltage at point K to decay sufficiently so that the next positive going input will transfer enough charge through C_1 to reliably toggle the flip flop. The maximum guaranteed toggle frequency of the flip flop is 15 MHz with rise and fall times of 9 ns, down time of 29 ns, and 800 mV amplitude. The typical toggle frequency is above 20 MHz when driven from a gate with sharp rise and fall times. Maximum toggle frequency is very dependent upon clock rise time and clock amplitude. This dependence is caused by the variable sensitivity of the flip flop with input rise time changes. Refer to the following section on descriptive curves for MECL flip flops for data showing this relationship.

Typical propagation delay time is 7 ns while nominal rise and fall times are 7 ns and 8 ns respectively. Power dissipation is about 85 mW at V_{EE} = -5.2 V.

DESCRIPTIVE CURVES FOR MECL FLIP-FLOPS

The following data is most helpful to the designer in understanding the characteristics of

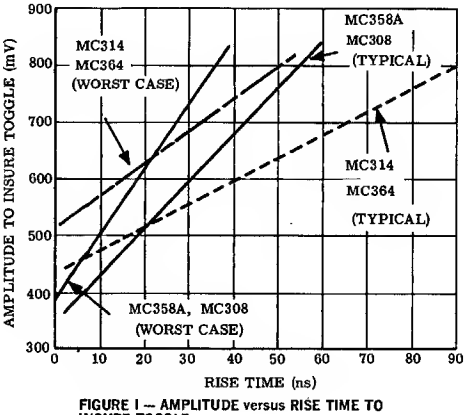


FIGURE I — AMPLITUDE versus RISE TIME TO INSURE TOGGLE

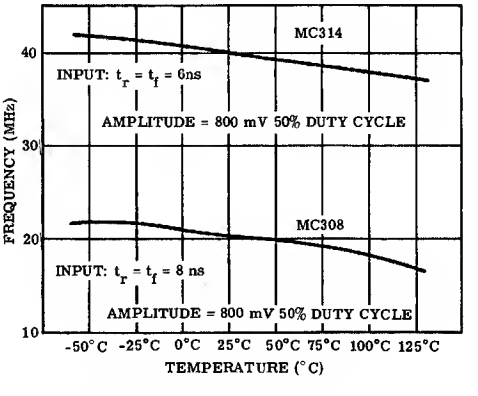
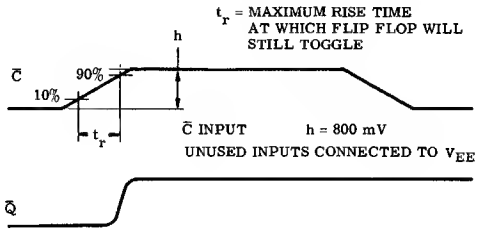


FIGURE II — TYPICAL TOGGLE FREQUENCY versus TEMPERATURE

continued

MECL flip flops. As may be seen from the data, typical characteristics can be much better than those specified for worst case. In fact, typical data usually runs about 30% better than worst case. For example, the distribution of characteristics is wide enough that for fast rise and fall times some of the MC314 flip flops will toggle reliably at 50 MHz. The curves are self-explanatory and include the test conditions for data shown in Figures I, II, III, IV, and V.



90% OF THE DEVICES WILL TOGGLE AT RISE TIMES EQUAL TO OR LESS THAN THAT SHOWN

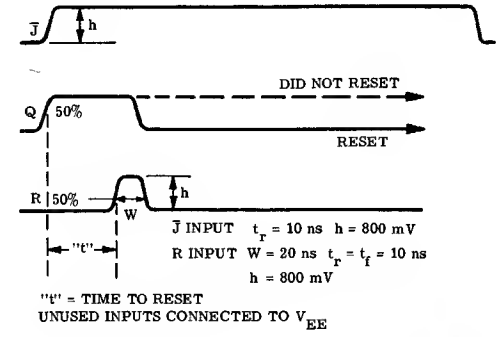
FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	60ns		70ns		90ns
MC364		60ns	70ns	85ns	
MC308	40ns		45ns		70ns
MC358A MC358		40ns	45ns	50ns	

NOTE: FOR WORST CASE DESIGN t_r SHOULD BE:

MC314, MC364: $t_r < 50$ns @ 800mV

MC308, MC358A: $t_r < 35$ns @ 800mV

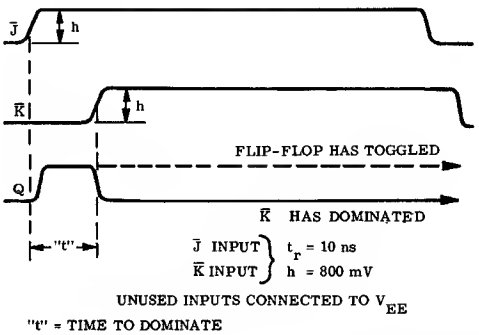
FIGURE III — MAXIMUM RISE TIME TO TOGGLE TEST



THE MAXIMUM VALUES ARE GIVEN BELOW WITH A 90% CONFIDENCE LEVEL

FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	2ns		1ns		1ns
MC364		6ns	3ns	7ns	
MC308	22ns		13ns		33ns
MC358A		18ns	9 ns	22ns	

FIGURE IV — MAXIMUM TIME TO RESET TEST

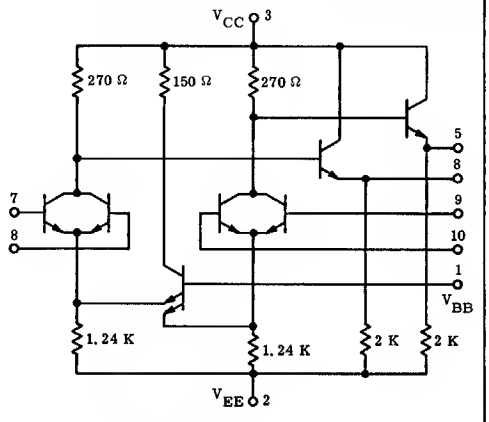


THE MAXIMUM VALUES ARE GIVEN BELOW WITH A 90% CONFIDENCE LEVEL

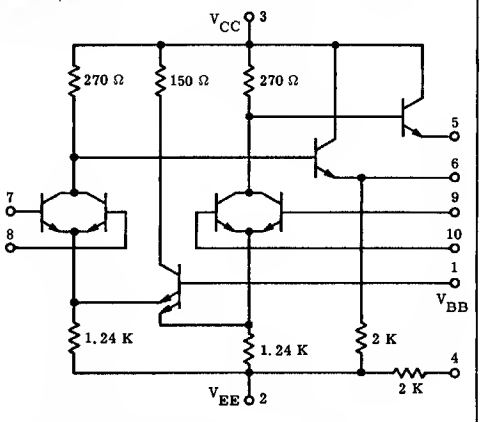
FLIP FLOP	-55°C	0°C	25°C	75°C	125°C
MC314	20 ns		21 ns		16 ns
MC364		30 ns	32 ns	35 ns	
MC308	30 ns		33 ns		41 ns
MC358A		20 ns	21 ns	26 ns	

FIGURE V — MAXIMUM TIME TO DOMINATE TEST

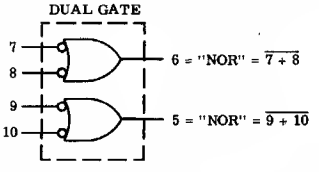
DUAL 2 INPUT NOR, BOTH PULL-DOWN RESISTORS: MC309, MC359



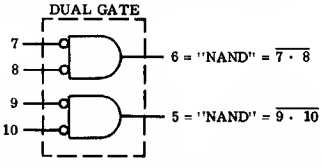
DUAL 2 INPUT NOR, ONE PULL-DOWN RESISTOR, ONE OPTIONAL: MC310, MC360



POSITIVE LOGIC
When V_H is defined as a logical "1" and V_L as a logical "0" the "NOR" function is performed:



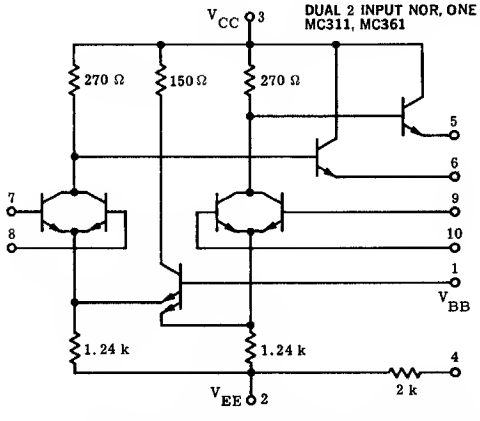
NEGATIVE LOGIC
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "NAND" function is performed:



Use of the Dual 2-input NOR gate will usually result in a lower "can count" i.e. the total number of integrated circuits used in a given system. Note that pin 1 the bias driver input is equivalent to two standard loads due to the double emitter output. Typical propagation delay is 7 ns, with a rise time of 6 ns and fall time of 7.5 ns at 25°C. Nominal power dissipation is 55 mW.

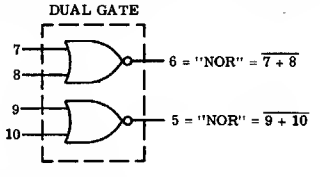
This gate is identical to the MC309, MC359, except that pin 4 allows the option of a pull-down resistor or power savings for the output on pin 5. Typical power dissipation with pin 5 connected to 4 is 55 mW, while it is only 43 mW at V_{EE} = -5.2 V without the pull down resistor. Typical propagation delay is 7 ns. Nominal rise and fall times are 6 ns and 7.5 ns respectively at room temperature.

DUAL 2 INPUT NOR, ONE OPTIONAL PULL-DOWN RESISTOR: MC311, MC361

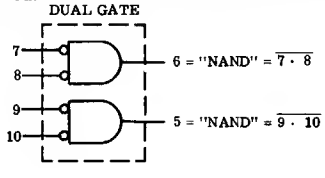


This gate is useful where wire-OR'd outputs are a savings. Both outputs are normally without pull-down resistors which reduces the nominal power dissipation to 31 mW. If the pull-down resistor on pin 4 is used, the nominal dissipation increases to 43 mW. Note the rules governing the wired-OR outputs under General Rules for MECL shown on a previous page. Propagation delay is typically 7 ns with 6 ns rise and 7.5 ns fall times at room temperature.

POSITIVE LOGIC
When V_H is defined as a logical "1" and V_L as a logical "0" the "NOR" function is performed:

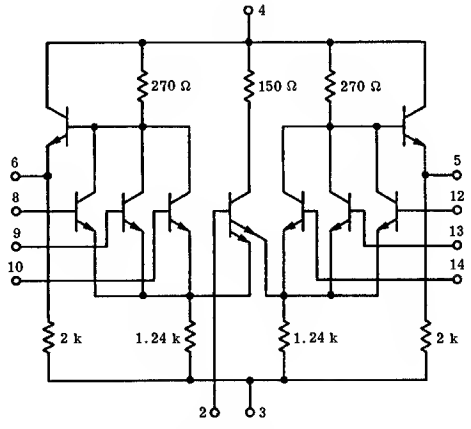


NEGATIVE LOGIC
Inversely, when V_H is defined as a logical "0" and V_L as a logical "1" the "NAND" function is performed:

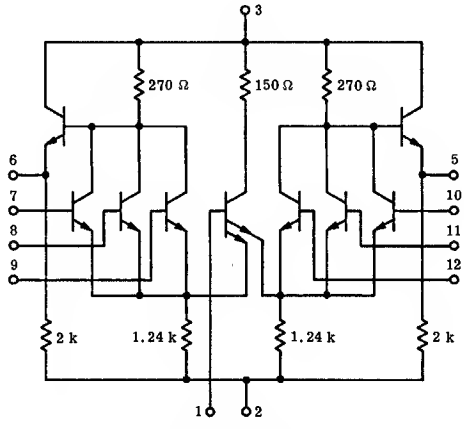


DUAL 3 INPUT NOR: MC312, MC362

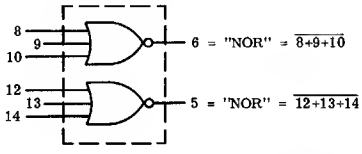
MC312F, MC362F



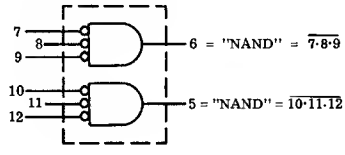
MC312G, MC362G



Positive Logic

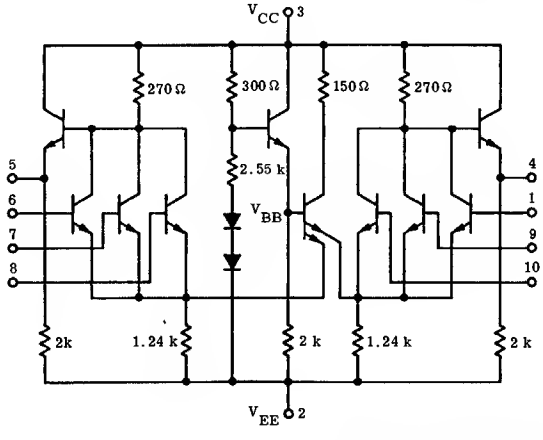


Negative Logic

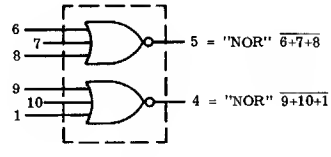


These circuits are preferred wherever three-input gates provide a savings. The F model is available in a 14-pin flat package while the G model number indicates a 12-pin TO-5 package. The typical power dissipation is 55 mW. Nominal delay time is 7 ns with output rise and fall times of about 7 ns.

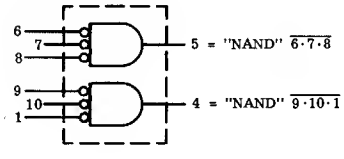
DUAL 3 INPUT NOR WITH BIAS DRIVER: MC312A, MC362A



Positive Logic

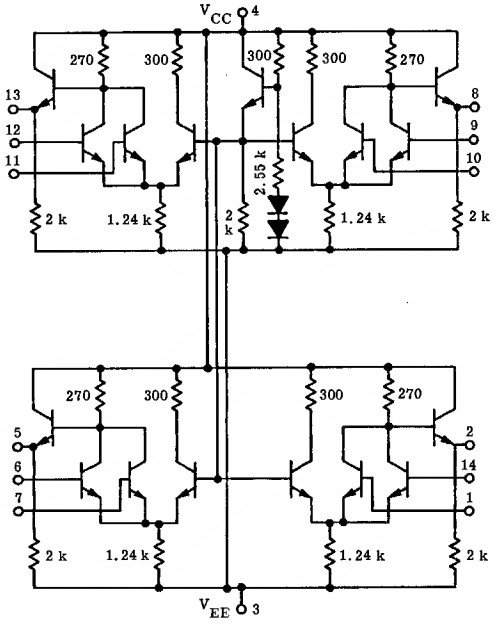


Negative Logic



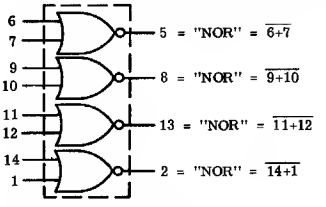
The MC312A, MC362A is essentially the same as the MC312, MC362 except that a bias driver is included on the same monolithic chip, allowing the circuit to be mounted in a 10-pin TO-5 can. Typical characteristics are: power dissipation 72 mW, propagation delay time 8.5 ns and rise and fall times of 9 ns.

QUAD 2 INPUT NOR WITH BIAS DRIVER: MC313F, MC363F



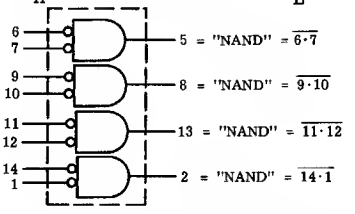
POSITIVE LOGIC

V_H is defined as logical "1", V_L as logical "0"



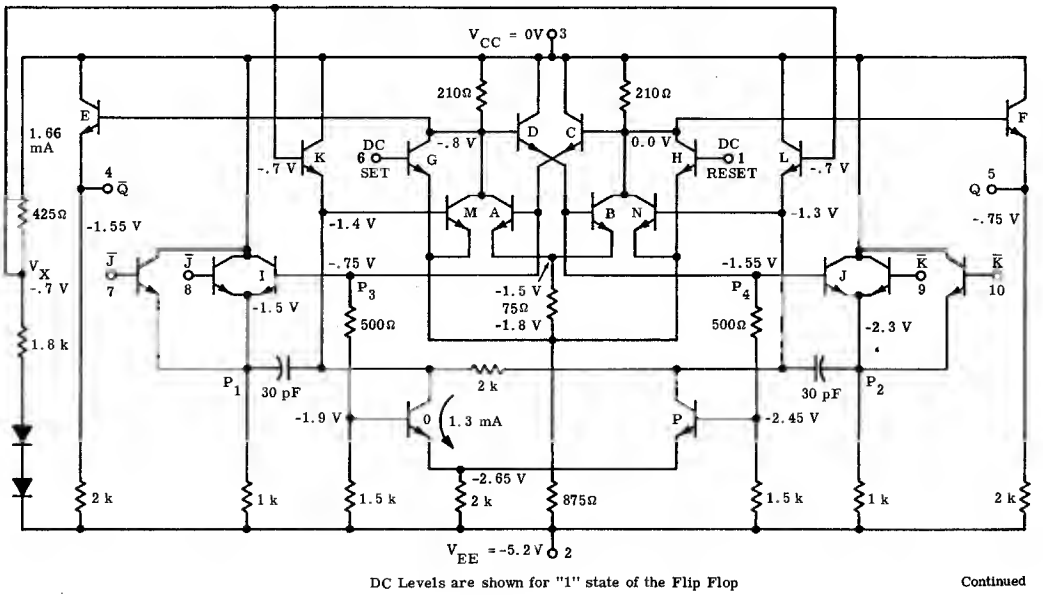
NEGATIVE LOGIC

V_H is defined as logical "0", V_L as logical "1".



The MC313F is available only in the 14-pin flat package due to pin-out limitations of the TO-5 configuration. This multiple function gate may be used to advantage in reducing the can count in a system. Typical power dissipation is 125 mW. Nominal propagation delay time is 7 ns, with a rise time of 6 ns and a fall time of 7.5 ns. The built-in bias driver not only saves a pin but effectively adds to the noise immunity because it sees a fixed load.

J-K FLIP-FLOP, DC R-S; HIGH SPEED, BUFFERED OUTPUTS: MC314, MC364



DC Levels are shown for "1" state of the Flip Flop

Continued

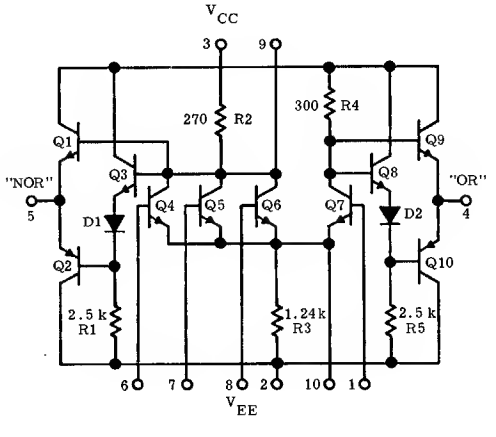
The MC314, MC364 utilizes 20 transistors and two junction capacitors in a high-speed design that guarantees a minimum toggle frequency of 30 MHz at room temperature while typical toggle frequency is 40 MHz at room temperature. Typical characteristics are: power dissipation 115 mW, propagation delay time 12 ns, rise time 13 ns, and fall time 12 ns.

The adjacent schematic shows the nominal D.C. levels for the flip flop in the "1" state, i.e. Q = -0.75 V. Transistors A through H function the same way as in the MC308, MC358A. A and B form the bi-stable element with feedback through D and C. Transistor G sets the flip flop to a "1" while H resets to "0". Transistors E and F buffer the outputs and prevent noise from feeding back into the flip flop from external sources. Transistor I is turned on ensuring that point P_1 is at -1.5 volts. This inhibits a normal MECL $\overline{J}$ input from affecting the state of the flip flop. A high $\overline{J}$ input would have no effect since P_1 is already at -1.5 V.

The K inputs are enabled and a positive going MECL level will couple charge through the 30 pF capacitor and raise the emitter of L to about -0.9 V at which point it is clamped by N which is forward biased and causes the flip flop to change state. As soon as the flip flop changes state, P_4 is raised from -1.55 V to -0.75 V which switches the constant current (1.3 mA) from transistor O to transistor P. This constant current discharges the 30 pF capacitor in about 10 ns. It is seen that the flip flop may be set or reset very soon after a $\overline{J}$ or $\overline{K}$ input has been received due to the rapid discharge of the capacitor. The 30 pF capacitor and the 1 k resistor also form a time constant that requires a minimum down time on a clocking waveform. The 30 ns time constant requires about 8 ns to decay from -1.5 V to -2.3 V with nominal values of R and C. This requires a down time of at least 10 ns at the 10% levels of the clocking waveform. The voltage V_X is internally generated to track with MECL levels over temperature and power supply variations. Transistors K and L are very lightly turned on. One of them, depending upon the state of the flip flop, supplies current for the constant current source employing transistors O and P and the 2 k resistor to V_{EE}. The 2 k resistor between collectors provides a 50 μa pull-down current for either K or L depending upon which is not providing the 1.3 mA discharge current.

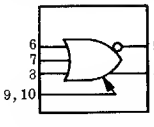
Logically, the MC314, MC364 design is identical with that of the MC308, MC358A. The electrical characteristics have some variations besides maximum toggle frequency. These are illustrated in the section containing MECL flip flop curves.

LINE DRIVER AND CAPACITANCE DRIVER: MC315, MC365



The MC315, MC365 is most useful whenever high speed digital information with little allowed degradation is to be transmitted over long distances without noise pickup. This circuit will drive coax of 50Ω impedance or higher with degradation dependent only upon line losses. Also high values of capacitance may be driven with good rise and fall times.

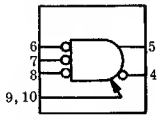
POSITIVE LOGIC - Simultaneous "OR"/"NOR"; V_H is defined as logical "1", V_L as logical "0".



5 = "NOR" = $\overline{6+7+8}$ = $\overline{6}\cdot\overline{7}\cdot\overline{8}$

4 = "OR" = $6+7+8$ = $\overline{\overline{6}\cdot\overline{7}\cdot\overline{8}}$

NEGATIVE LOGIC - Simultaneous "AND"/"NAND"; V_H is defined as logical "0", V_L is logical "1".



5 = "NAND" = $\overline{6\cdot7\cdot8}$ = $\overline{6}+\overline{7}+\overline{8}$

4 = "AND" = $6\cdot7\cdot8$ = $\overline{\overline{6}+\overline{7}+\overline{8}}$

The gate is a 3-input OR, NOR with bias voltage normally applied to pin 1. Unused inputs must be returned to -5.2 V. The outputs, pins 4 and 5, have active devices to both pull-up and pull-down the load as necessary. For a "1" level output (-0.75 V), the NPN output transistor is turned on giving the low output impedance of an emitter follower to charge any line capacitance. Very low impedance is also provided by the PNP emitter follower to discharge any line capacitance.

Continued

Maximum power dissipation with both outputs loaded to ground with 50Ω is 240 mW, which for maximum reliability requires a case temperature of 125°C maximum rather than 125°C ambient. With only one output loaded, 50Ω to ground, maximum power dissipation is 170 mW. Reducing the single load to 100Ω further decreases dissipation to 110 mW.

For a load of 50Ω and .001μF to ground, the propagation delay is typically 16 ns at room temperature while rise and fall times are about 20 ns. With 50Ω coax terminated in a 50Ω resistor, rise time is typically 15 ns and fall time 20 ns with propagation through the device of about 14 ns.

If the device is used as a capacitance driver, output rise and fall times and propagation delay times depend upon the value of capacitance. Typical curves showing this dependence are drawn below in figures A, B, C, and D. A 10Ω resistor was put in series with the load capacitor to prevent overshoot and ringing on the output waveform. The 10Ω resistor damps the series L-C circuit formed by lead inductance and the lumped capacitance. Without the resistor, overshoot may be about 300 mV depending upon the size of the capacitor. More information on driving lines from MECL outputs may be found in application note AN-187.

Figure E illustrates graphically definitions for rise, fall, and delay times.

For gate loaded 50Ω to ground with variable capacitance in parallel, figures F and G show output rise, fall, and delay times.

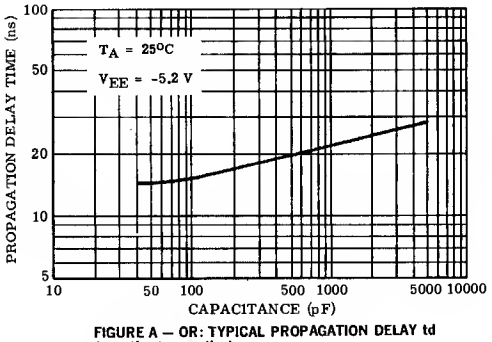


FIGURE A — OR: TYPICAL PROPAGATION DELAY t_d (negative to negative)

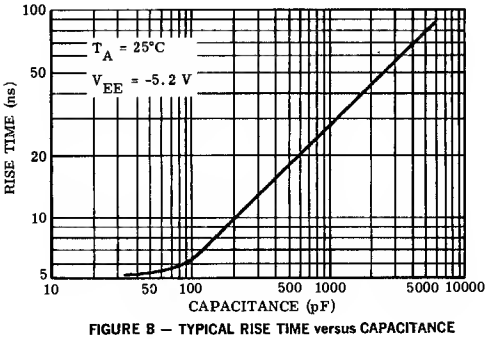


FIGURE B — TYPICAL RISE TIME versus CAPACITANCE

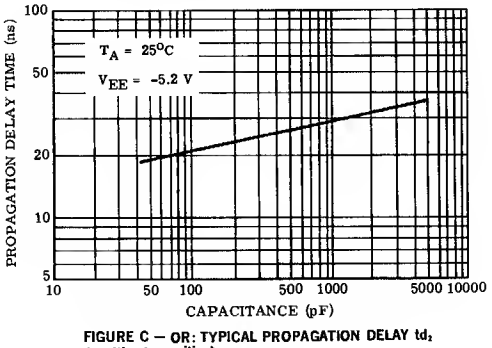


FIGURE C — OR: TYPICAL PROPAGATION DELAY t_{d_2} (positive to positive)

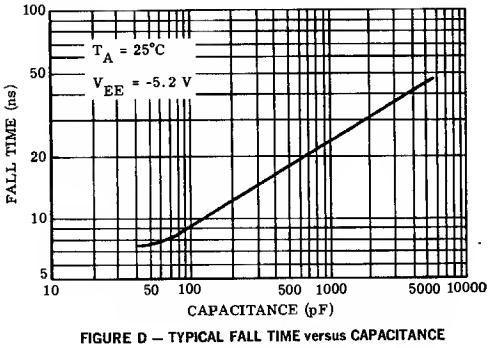


FIGURE D — TYPICAL FALL TIME versus CAPACITANCE

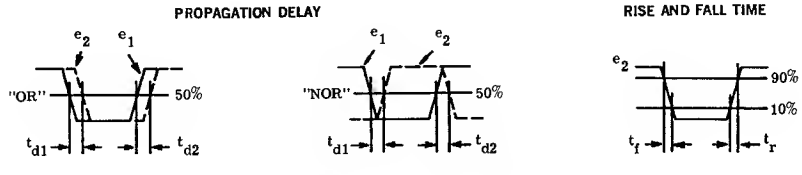


FIGURE E — RISE, FALL AND DELAY INTERVALS

Continued

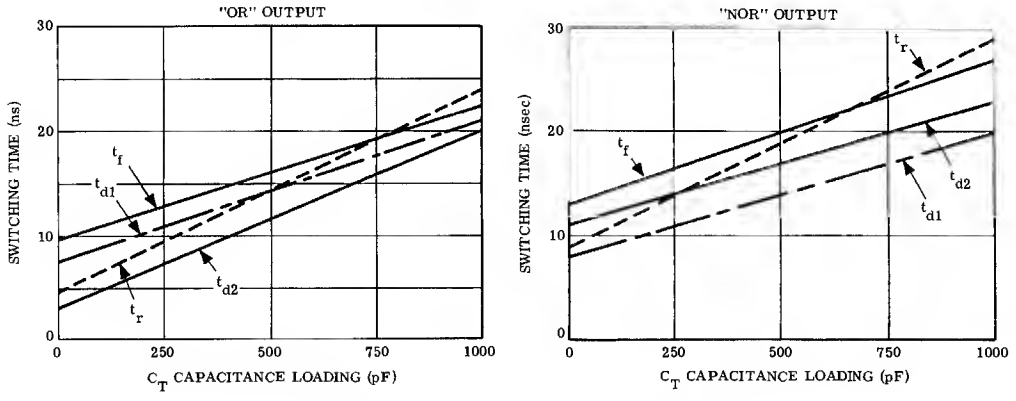


FIGURE F — SWITCHING CHARACTERISTICS OF MC315, MC365

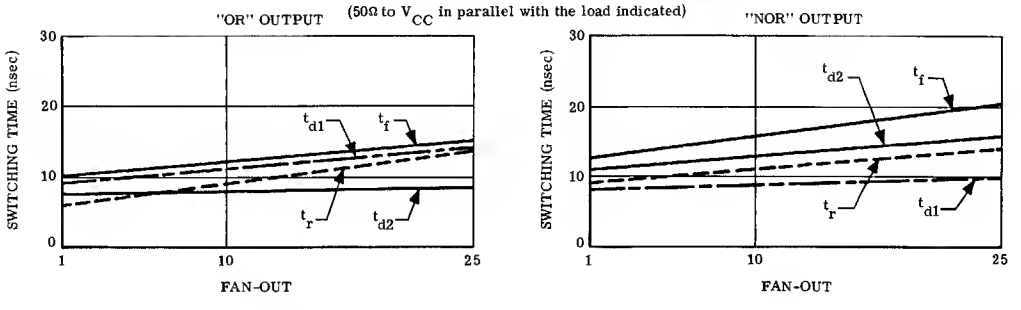
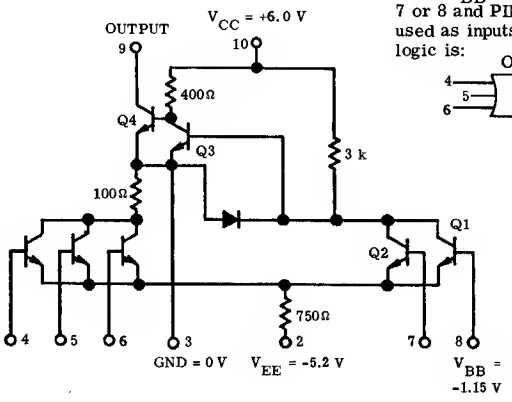
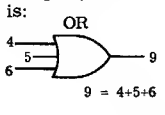


FIGURE G — TYPICAL SWITCHING CHARACTERISTICS OF MC315, MC365

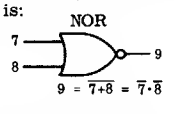
LAMP DRIVER: MC316, MC366



When V_{BB} is applied to PINS 7 or 8 and PINS 4, 5 and 6 are used as inputs; the resultant logic is:



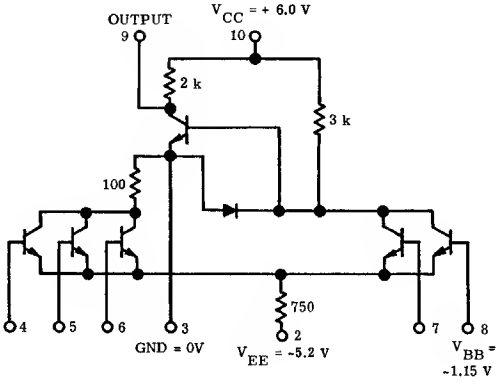
When V_{BB} is applied to PINS 4, 5 or 6, and PINS 7 and 8 are used as inputs; the resultant logic is:



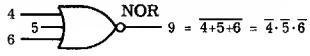
The Lamp Driver operation is the same as that of a regular gate except for the output circuitry which presents saturated logic levels. The current through the 3 k resistor is either switched through the base of Q_3 or transistors Q_1 and Q_2. Q_4, the output transistor, may then be used to turn an indicator light on or off. The diode becomes useful if the gate is to be used as a high speed switch by preventing saturation of Q_1 and Q_2.

Q_4 will sink a maximum of 100 mA at 25°C and 50 mA at 125°C. The maximum V_{sat} is 1.0 V at 100 mA. Typical V_{sat} is 0.75 V at 100 mA with a V_{CC} of 4 V to 6 V. Maximum power dissipation is 235 mW at 6 V and 100 mA sink current.

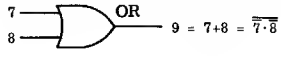
LEVEL TRANSLATOR MECL TO DTL: MC317, MC367



When V_{BB} is applied to PINS 7 or 8, and PINS 4, 5 and 6 are used as inputs; the resultant logic is:



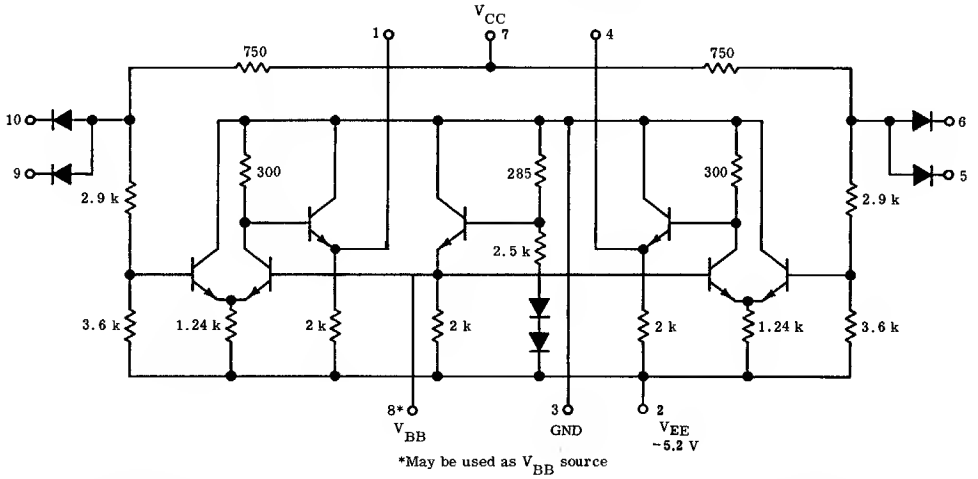
When V_{BB} is applied to PINS 4, 5 or 6, and PINS 7 and 8 are used as inputs; the resultant logic is:



The primary function of this gate is to act as a high speed interface between MECL logic levels and those of saturated logic. Operation is identical to that of the MC316, MC366 Lamp Driver except for the elimination of the output driver transistor.

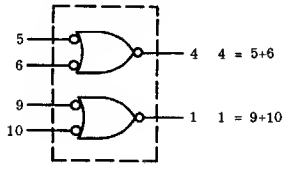
Maximum saturation voltage of 0.45 V at 25°C is specified for a sink current of 10 mA, while typical V_{sat} is 0.25 V. The output voltage at no load is essentially V_{CC}. Turn on and turn off times are a maximum of 30 ns and 35 ns respectively while worst case power dissipation is 75 mW over the full temperature range.

LEVEL TRANSLATOR DTL TO MECL: MC318, MC368



*May be used as V_{BB} source

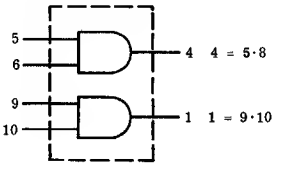
NEGATIVE LOGIC



LOGIC SPECIFICATION

By applying DTL input logic levels as defined by logical "0" at 0.4 V and logical "1" at 5.0 V, corresponding MECL outputs are obtained as defined by logical "0" at -1.55 V and logical "1" at -0.75 V.

POSITIVE LOGIC

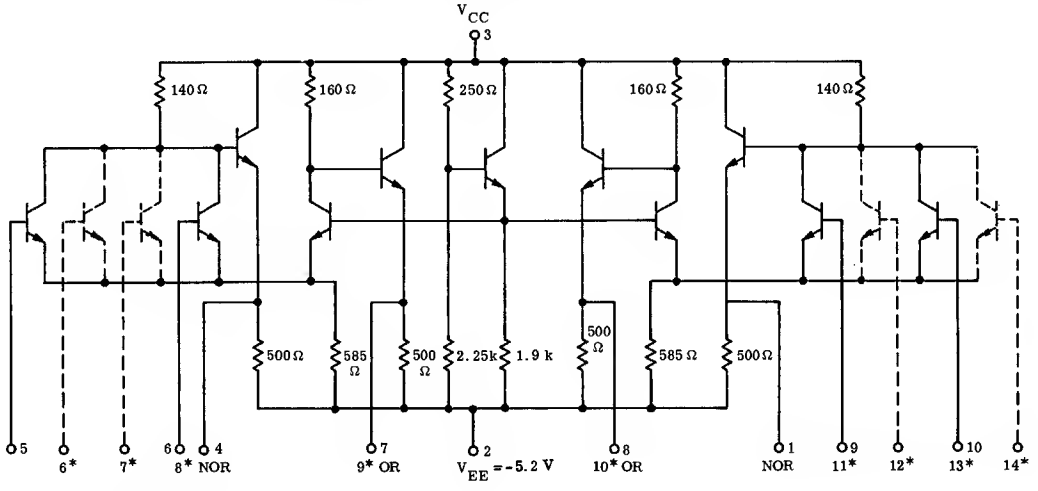


Continued

This device is used wherever a high-speed level translator from saturated logic to MECL is required. Turn on and turn off times are about 15 ns with output rise time and fall time nominally 7.5 ns. Maximum power dissipation is 120 mW over the temperature range. The saturated logic input levels should switch from about +0.5 V to + 5.0 or + 6.0 V for the above specifications.

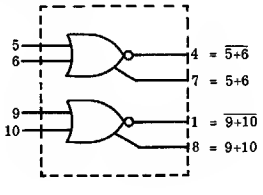
The dual translator operation is as follows: If inputs 5 and 6 are high, the logic input of the respective MECL gate receives a high level through the voltage divider. The OR output of the first MECL gate on pin 4 will then go high. The second translator functions in the same manner for inputs on pins 9 and 10 and an output on pin 1. The device contains a built-in bias driver that compensates for voltage and temperature variations. This reference voltage is available to drive additional gates. A maximum fan-out of 23 is available. Both translators perform the positive AND logic function.

MC369G DUAL-2 OR, NOR CLOCK DRIVER AND HIGH-SPEED GATE
MC369F DUAL-4 OR, NOR CLOCK DRIVER AND HIGH-SPEED GATE



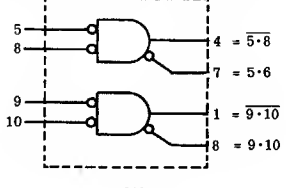
* MC369F ONLY

POSITIVE LOGIC
V_H is defined as logical "1", V_L as logical "0".



MD369G

NEGATIVE LOGIC
V_H is defined as logical "0", V_L as logical "1".



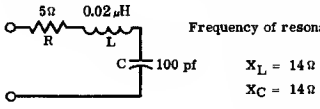
MD369F

The Clock Driver is a very low output impedance device (about 5Ω) and exhibits very fast rise and fall times. Because of its low output impedance and fast rise times, precautions must be taken to reduce ringing in circuits employing the device. The device will fan-out to one or two flip flops ($\overline{J}$ and $\overline{K}$ tied together) with a typical rise time of less than 4 ns. Also, a fan-out to 20 flip flops may be achieved with typical rise times of less than 9 ns.

Operation of the gate is the same as a standard MECL gate with the exception of lower resistance values and higher power dissipation. Typical characteristics at a fan-out of 10 MECL gate loads are: rise time 4.0 ns, fall time 5.0 ns, propagation delay time 5 ns, and power dissipation 240 mW.

Continued

Considering that in a clock driver application, a flip flop may be inhibited with a minimum "1" level and that overshoot may appear on a maximum "1" level clock, worst case allowable overshoot is only 100 mV over the temperature range. For room temperature applications overshoot should be limited to 150 mV. If a lumped capacitance load is added to the clock driver output, overshoot and ringing will be noted. The following is a simplified equivalent circuit for the clock driver output where: R = incremental output impedance of the emitter follower. L = the inductance of 1" of wire. C = the capacitance of 10 flip flop inputs with $\overline{J}$ and $\overline{K}$ tied together.



Frequency of resonance ≈ 113 MC

X_L = 14Ω

X_C = 14Ω

This represents an underdamped series R-L-C circuit and overshoot will be a problem when a step function is applied to the input of the circuit. The following method has been found satisfactory for reducing overshoot to 100 mV or less: (1) Keep the output lead of the device as short as possible, (2) Tap off from the output lead with a resistor of appropriate value to each input being clocked, (3) Keep all devices being clocked as close as possible to the clock driver, (4) If overshoot is still a problem, it may be reduced by 30% to 50% by paralleling two outputs, i.e. two OR's or two NOR's from the same can. This reduces by half the current flowing through an output lead.

The following data in the table are given as a guideline for selecting the proper resistor to be used in series with each flip flop input. Power supplies were bipassed to ground and all loading flip flops were kept within 3 inches of the clock driver.

TABLE OF OVERSHOOT AND RISE-TIME

VS. RESISTANCE AND FAN-OUT

FO = 1 R = 0Ω

S		P	
OS	t_r	OS	t_r
50 mV	3.4 ns	25 mV	3.4 ns

FO = 2 R = 0Ω

S		P	
OS	t_r	OS	t_r
115 mV	3.4 ns	70 mV	3.4 ns

FO = 3 R = 0Ω

S		P	
OS	t_r	OS	t_r
175 mV	3.5 ns	105 mV	3.4 ns

FO = 5 R = 200Ω

S		P	
OS	t_r	OS	t_r
120 mV	5.5 ns	95 mV	5.5 ns

FO = 10 R = 200Ω

S		P	
OS	t_r	OS	t_r
180 mV	5.9 ns	140 mV	5.6 ns

FO = 10 R = 330Ω

S		P	
OS	t_r	OS	t_r
100 mV	7.1 ns	75 mV	6.9 ns

FO = 15 R = 330Ω

S		P	
OS	t_r	OS	t_r
135 mV	7.3 ns	100 mV	7.1 ns

FO = 10 R = 470Ω

S		P	
OS	t_r	OS	t_r
50 mV	8.4 ns	40 mV	8.4 ns

FO = 20 R = 470Ω

S		P	
OS	t_r	OS	t_r
100 mV	8.6 ns	70 mV	8.3 ns

FO = fan-out of clocked flip-flops

S = single gate output

P = paralleled gate outputs (from same can)

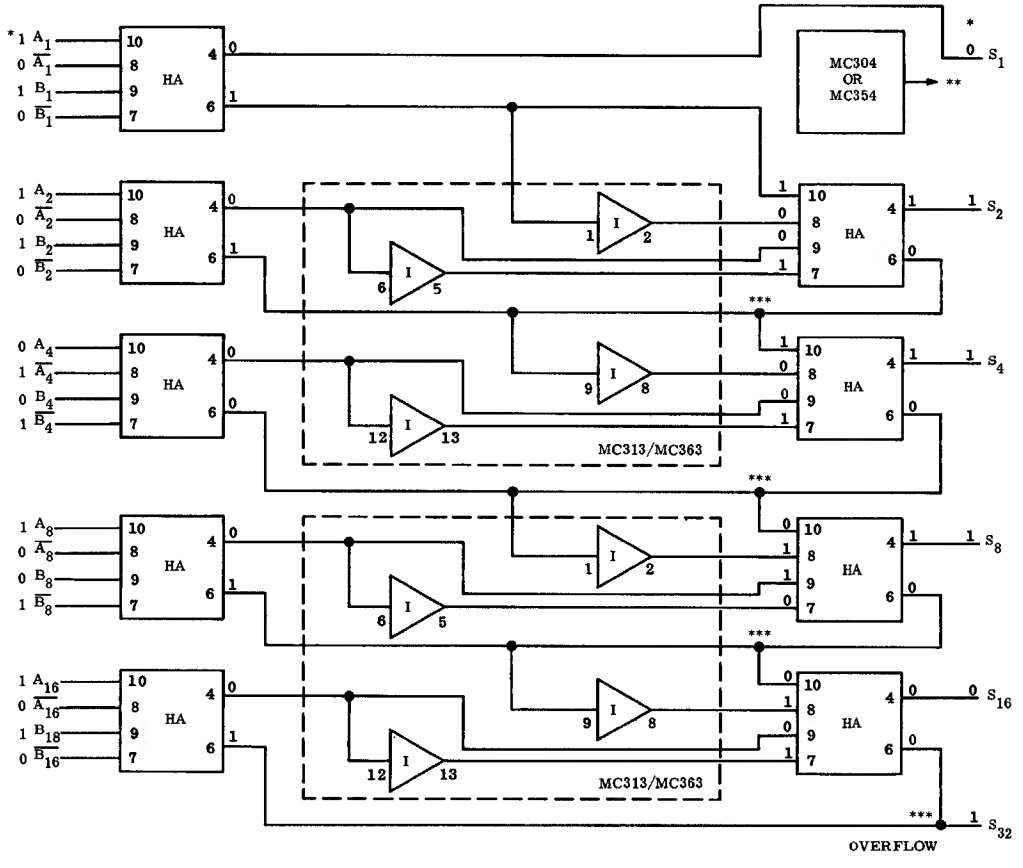
OS = overshoot in millivolts

t_r = rise-time in nanoseconds at input to a flip-flop

MECL SYSTEM APPLICATIONS

This section of sample applications of MECL is included to illustrate the use and versatility of this family. Note the short propagation times obtained. Also additional gates are saved by using the wired-OR feature of MECL.

MECL ASYNCHRONOUS PARALLEL FIVE BIT ADDER



The table illustrates the addition of two 5 bit binary numbers. The subscripts give the decimal equivalent weights of the binary bits. Logic levels for the example are shown in the logic diagram.

TYPICAL EXAMPLE

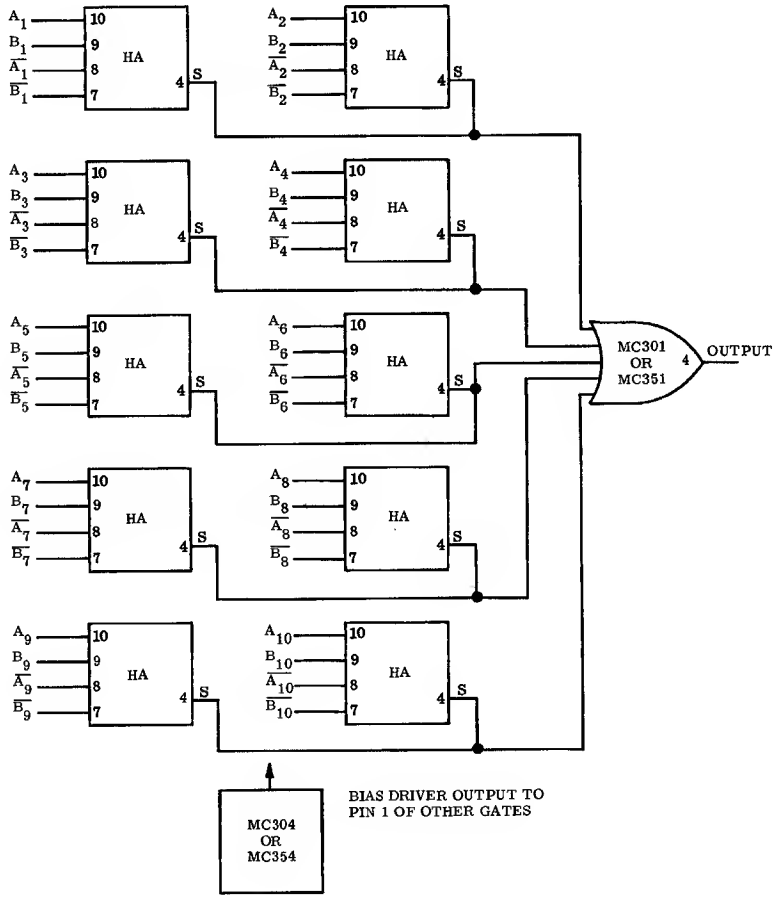
"A" AUGEND		"B" ADDEND		"S" SUM		"C" CARRY	
A_1	1	B_1	1	S_1	0	C_1	1
A_2	1	B_2	1	S_2	1	C_2	1
A_4	0	B_4	0	S_4	1	C_4	0
A_8	1	B_8	0	S_8	1	C_8	0
A_{16}	1	B_{16}	1	S_{16}	0	C_{16}	1

DEFINITIONS:
HA = Half Adder MC303 or MC353. A logical "1" is defined as a relatively high level (-.75 V). A logical "0" is defined as a relatively low level (-1.55 V).

NOTE: The inverters are obtained from 2-quad two-input gates. If desired, 4-dual two-input gates may be used instead of the 14-pin MC313/MC363.
"Can Count" = 9 Half Adders, 2 Quad 2-input gates, 1 Bias Driver = 12 "cans".
The 5-bit adder requires 9 gate delays for a carry to ripple through from the first Half Adder to the overflow output. The total propagation delay time is approximately 60 ns.

*Logic Levels are for the example shown in the table.
**The Bias Driver connects to each gate requiring external bias.
***Outputs are wire OR'd together.

ASYNCHRONOUS 10-BIT MECL COMPARATOR
(Employing the HALF-ADDER as an exclusive OR)



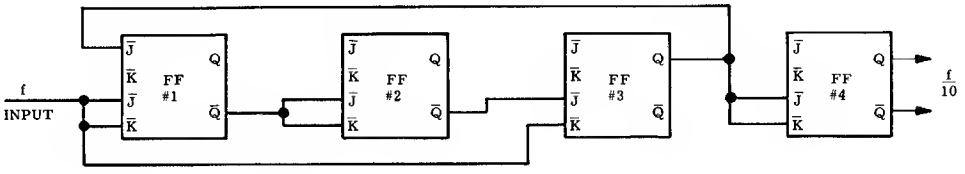
HALF ADDER Truth Table

Pin #	A	B	$\overline{A}$	$\overline{B}$	OUT
	10	9	8	7	4
	Lo	Lo	Hi	Hi	Lo
	Lo	Hi	Hi	Lo	Hi
	Hi	Lo	Lo	Hi	Hi
	Hi	Hi	Lo	Lo	Lo

This circuit employing only 12 devices indicates asynchronously whether or not the data from two sources (A and B) agree. If any one of the Half Adder gates (HA) has a pair of input bits that are different, the gate will have a high level output. The Half Adders are wire-OR'd together two at a time resulting in five outputs which drive a 5-input OR gate. The circuit output will be high if any datum from source A disagrees with the corresponding datum from source B.

The circuit has many uses such as enabling the step counting of a register until its output agrees with a given input. Total propagation delay time from input to output is approximately 15 ns. This high speed is an important asset in fast analog to digital conversion. As many bits as desired may be compared with similar propagation delay time by wire OR'ing the output of another 5-input OR with the one shown or by using an expandable gate instead of an MC301 or MC-351.

MECL ÷ 10 COUNTER

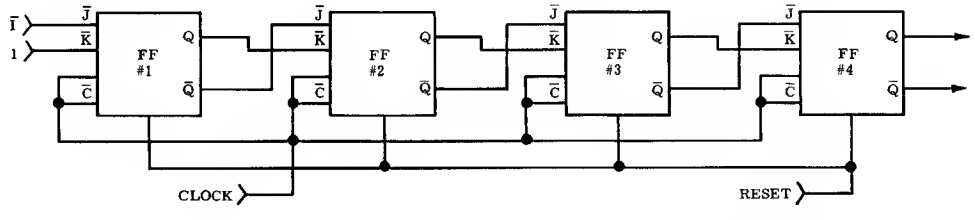


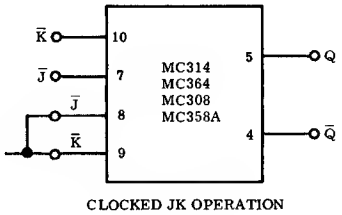
STATE #	FF #1	FF #2	FF #3	FF #4
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	1
5	0	0	0	1
6	1	0	0	1
7	0	1	0	1
8	1	1	0	1
9	0	0	1	0
10	0	0	0	0

NOTE:
1. A positive going $\overline{J}$, all other inputs to FF low, sets FF to "1".
2. A positive going $\overline{K}$, all other inputs to FF low, sets FF to "0".
3. In going from state 4 to 5, the "1" from FF 3 is fed back to the $\overline{J}$ input of FF 1 while the clock waveform is still high and inhibiting the flip flop. If the up-time of the clock is too short, the $\overline{J}$ input may set FF 1 to the "1" state causing an error.
4. FF 2 and 4 are connected in the toggle mode and simply divide by two.

The main advantage of MECL counters (besides speed), is that any desired count may be obtained without additional gates. The maximum input frequency (f) of the configuration shown is about 15 MHz, without selection of units. If MC314, MC364 flip flops are used and FF 4 is put first in the chain (yielding f/2); inputs of 30 MHz may be employed. The output in the second case is not symmetrical which may be a disadvantage. Further information on counters both clocked and asynchronous may be found in AN-194 and AN-257.

MECL 4-BIT SHIFT REGISTER





CLOCKED JK OPERATION

FLIP FLOP Truth Table

INPUT STATE	$\overline{J}$	$\overline{K}$	$\overline{C}$	Q^{n+1}
	ø	ø	0	Q^n
1	0	0	1	$\overline{Q^n}$
2	0	1	1	1
3	1	0	1	0
4	1	1	1	Q^n

continued

Information received in a shift register will normally be of input state 2 or 3 as shown in the truth table, i.e. inputs of opposite levels. It is seen from the table that the level of the $\overline{K}$ input will be stored in the flip flop, after a dynamic clock, and appear at the Q output. After the first flip flop in the shift register, changes state, the $\overline{J}$ and $\overline{K}$ inputs of the second receive their data. Since the "up time" of a clock waveform is longer than the propagation delay time of a flip flop, a following flip flop is inhibited while the $\overline{J}$ and $\overline{K}$ inputs may be changing levels. Since propagation delay is of no importance, it appears that the maximum shift frequency is the same as the maximum toggle frequency. This is almost true with one exception: If the zero level from the previous flip flop into the $\overline{J}$ or $\overline{K}$ input is more positive than the zero level of the clocking waveform, then a small portion of the clock waveform will be inhibited. This reduces the effective amplitude of the clock. (Note the schematic of one of the flip flops shown previously.) Since maximum toggle frequency depends upon clock amplitude, a reduction in typical operating speed for a given flip flop may be seen. For good clock waveforms and amplitudes, shift frequency is essentially the same as minimum guaranteed toggle frequency.

The Reset input may be used to set every stage to zero if desired, or a combination of Set and Reset inputs may be used to obtain a given count prior to shifting. If the D.C. Set or Reset input is at a high level when the clock also goes high, an undesirable voltage spike will be transmitted to the flip flop output. Therefore, a flip flop should only be Set or Reset at other than clocking time, preferrably when the clock is high.

Another application of the shift register is that of a digital delay. A bit delay of n clock pulses may be obtained between the input and output of a shift register containing n flip flops. Also the output of a shift register may be fed back to the input to form a ring counter. One bit may be inserted in a ring counter and recirculated to form a simple bit time generator for clocking computer decisions.

MECL 70 MHz J-K FLIP-FLOP

INTRODUCTION

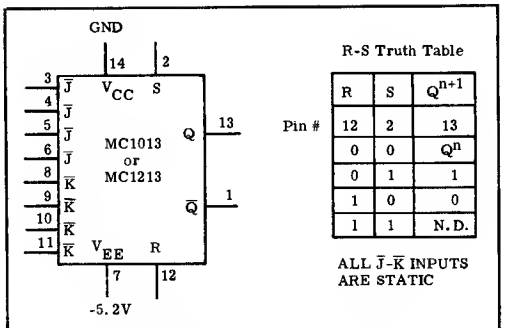
This note presents a thorough characterization of the MC1013/MC1213 $\overline{J}$-$\overline{K}$ flip-flop, which is a member of the new High Speed MECL II family. Both typical and worst case data for system design are given. The flip-flop is versatile in logic designs since four $\overline{J}$ and $\overline{K}$ inputs are provided. The typical operating speed of 85 MHz permits many high speed applications that were only possible with discrete components.

Figure 1 presents the truth tables and pin layouts for the flip-flop. The device is available in the dual in-line 14-pin plastic package (0°C to 75°C) and the 1/4" X 1/4" 14-pin ceramic flat package (-55°C to 125°C). Figure 2 is the device schematic with nominal resistor values. Circuit operation is the same as explained in AN-244 for the MC314/MC364 flip-flop.

The desired input levels are those of a standard MECL gate (see AN-244) i.e., a nominal voltage swing of 800 mV from -.75V to -1.55V at 25°C. Since capacitive coupling is internally employed, the device will accept large variations from the nominal values. In fact, 10 to 20 MHz may be added to the typical toggle frequency at 25°C by "overdriving" the clocked or toggle input with a 1.2V signal between the levels of about -0.4V and -1.6V and keeping the rise and fall times to 2 ns or less.

Figure 3 is the recommended circuit for driving the flip-flop from a pulse generator. For optimum performance, the lead length into and out of the 2N3959 must be kept short to prevent excessive overshoot. The 2N3959 is a 1.8 GHz device and gives good performance down to 1 ns rise and fall times. Output impedance is less than 20 Ω. This circuit closely approximates the output of the MC1023 clock driver which will be available in the first quarter of 1967. The MC1023 exhibits a typical rise time of 2.0 ns and fall time of 3.0 ns at a fanout of 10 (5 $\overline{J}$-$\overline{K}$ pairs) where lead lengths are kept to one inch or less. Each $\overline{J}$-$\overline{K}$ pair should have a separate input lead to the clock driver output if point to point wiring is used.

Other devices in the MECL family will also drive the MC1013/MC1213 satisfactorily at slower risetimes, resulting in slightly lower operating frequencies. The MC369G, MC1050, MC1051, MC1052, all exhibit typical risetimes of 4.0 ns and fall times of 5 ns at a fanout of 5 clocked flip-flops. The flip-flop itself makes a satisfactory driver with a typical output impedance of 15 Ω, risetime of 4 ns, and fall time of 5 ns at a small fanout.



R-S Truth Table

Pin #	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

ALL $\overline{J}$-$\overline{K}$ INPUTS ARE STATIC

Clocked $\overline{J}$-$\overline{K}$ Truth Table

Pin #	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	ø	ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	-	1	1	1
	1	0	1	0
	1	1	1	Q^n

ALL OTHER $\overline{J}$-$\overline{K}$ INPUTS AND THE R-S INPUTS ARE AT A "0" LEVEL

$\overline{J}_D$-$\overline{K}_D$ Truth Table

Pin #	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

ALL OTHER $\overline{J}$-$\overline{K}$ INPUTS AND THE R-S INPUTS ARE AT A "0" LEVEL

NOTES

1. N.D. stands for NOT DEFINED
2. *Any one of the $\overline{J}$ or $\overline{K}$ inputs may be used.
3. **Any $\overline{J}$ and $\overline{K}$ inputs may be tied together to form C_D eg. pins 6 and 8
4. -0.75V nominal is defined as a logic "1" or high level and -1.55V nominal is defined as a logic "0" or low level. $\overline{J}$ and $\overline{K}$ refer to static levels while $\overline{J}_D$, $\overline{K}_D$, C_D refer to dynamic positive-going transitions for a "1".
   A high level on a $\overline{J}$ input inhibits the flip-flop from being set by a $\overline{J}_D$ input. Likewise a "1" level on a $\overline{K}$ inhibits a $\overline{K}_D$ from resetting the flip-flop. The $\overline{J}$ and $\overline{K}$ inputs perform the "OR" function in preventing a $\overline{J}_D$ or $\overline{K}_D$ from setting or resetting the flip-flop.

FIGURE 1 — MECL II J-K FLIP FLOP LOGIC DIAGRAM AND TRUTH TABLES

MC1013/MC1213 CHARACTERISTICS

The following curves are most useful in describing the various parameters of the flip-flop under different operating conditions. The worst case data shown is conservative and may be used for system design purposes. If good system layout techniques are employed, the worst case system data observed will be better than that shown in the graphs. Poor system layout such as long inductive leads, high lumped values of capacitance, and unnecessarily large fanouts can reduce the typical operating speed considerably below 70 MHz.

Figure 4 illustrates the typical and worst case toggle frequency (or divide-by-two parameter) of the flip-flop. The guaranteed minimum toggle frequency of 70 MHz at 25 C is internally guard-banded by the manufacturer to prevent correlation problems with the customer. The toggle test is run with the circuit shown in Figure 3 with 800 mV input amplitude, less than 2.0 ns rise and fall times and a duty cycle of 50%. This test also assures a minimum allowed down and up time of 7.0 ns for the clocking waveform at 25°C (measured at the 50% levels). The worst case down or up time over the full temperature range is 9.0 ns. This corresponds to a worst case toggle frequency of 55 MHz at 125°C. The loading on the flip-flop has a negligible effect upon toggle frequency due to the emitter followers that isolate the flip-flop from the load. With the test input as stated above, a small percentage of the devices will toggle at 100 MHz. Slower rise and fall times will reduce this maximum frequency of operation. It should be noted that

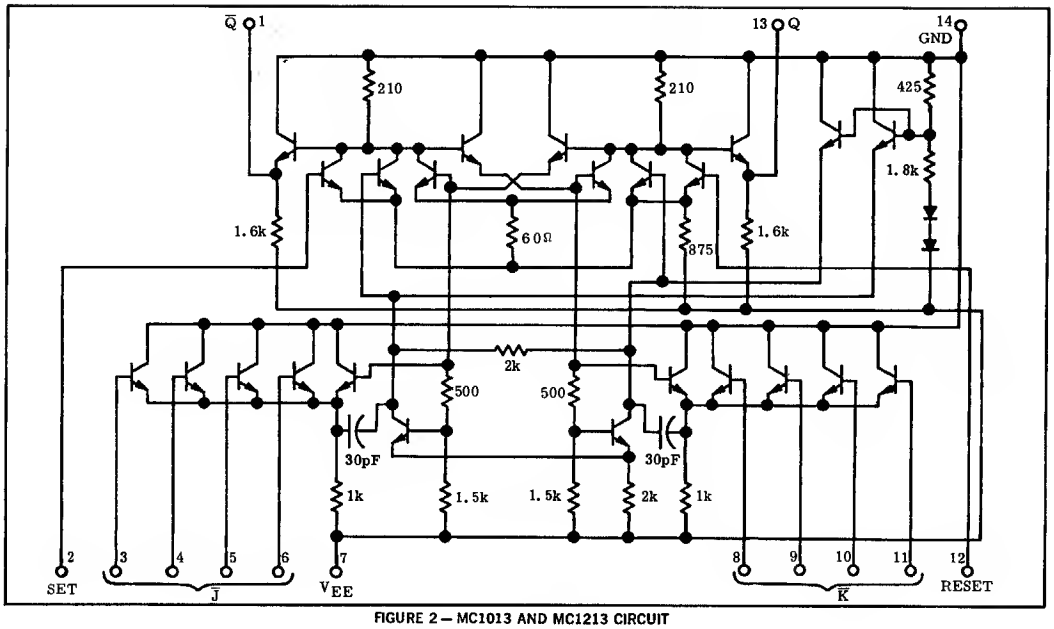


FIGURE 2 — MC1013 AND MC1213 CIRCUIT

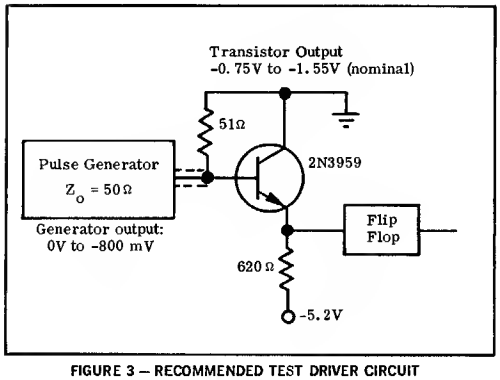


FIGURE 3 — RECOMMENDED TEST DRIVER CIRCUIT

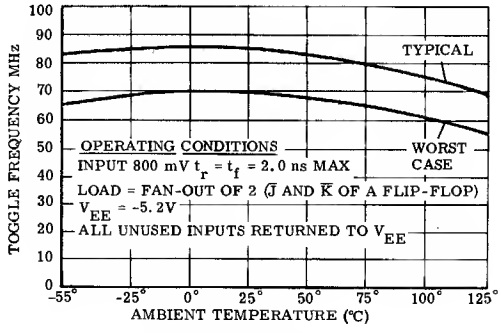


FIGURE 4 — TYPICAL AND WORST CASE TOGGLE FREQUENCY versus AMBIENT TEMPERATURE

a gate with 4 ns rise and fall times can do no better than a sine wave at 90 MHz.

The typical toggle frequency vs. V_{EE} curve, shown in Figure 5, illustrates the versatility of the MECL design that exhibits common mode rejection of V_{EE} supply variations. Toggle frequency changes very little for ±20% variations in supply voltage. The flip-flop appears as a nominal 215Ω resistive load to the power supply. Therefore, power dissipation is proportional to the square of V_{EE}. At a V_{EE} of -4V, power dissipation drops to a nominal 75 mW. At least 90% of the flip-flops will drive another device with V_{EE} varying from -3.0V to -8V at 25°C.

The minimum input amplitude required to toggle or clock the flip-flop at a given rise time is an important parameter. This measure of sensitivity varies with input rise time as shown in Figure 6. All flip-flops exhibit a slope of about 7.3 mV per ns as is shown for the typical flip-flop. The maximum variation in slope is ±20% which permits worst case design points to be guaranteed by the specification points shown in Figure 6. The worst case limit lines (for least sensitive devices and most sensitive devices) are obtained by changing the slope from that of the nominal flip-flop and leaving a guard-band that insures validity over the full temperature range. (See Figure 13 "Typical Sensitivity Variation VS. Temperature"). The specification points, tested on 100% of the devices, are: the flip-flop must not toggle on 300 mV input at 5.0 ns rise time and the flip-flop must toggle at 600 mV input at 20 ns rise time. These points are guard-banded to prevent any correlation problems. The worst case design points are: An input of 800 mV and greater than 100 ns rise time will not toggle the flip-flop. An input of 800 mV and less than 40 ns rise time will toggle the flip-flop. An input of 250 mV will not toggle the flip-flop, even at 0 ns rise time. These worst case values hold for the full temperature range of -55°C to 125°C.

Figure 7 illustrates typical and worst case propagation delay, rise, and fall times for a fanout of one clocked flip-flop (J and K tied together). The worst case curves are conservative and, therefore, recommended for system design at a fanout of two. t_{pd+-} stands for the propagation delay through the flip-flop from 50% of the positive going clock input to 50% of the negative going output. t_{pd++} is measured from 50% of the positive going clock input to 50% of a positive going output. All clock inputs and outputs are symmetrical and the results are the same regardless of which inputs or outputs are used in the measurements.

The typical and worst case delay, rise, and fall times vs. fanout of MC1000/MC1200 series gates are given in Figure 8. The MECL II gates exhibit less input capacitance than the MC300/MC350 series of MECL. Worst case data for 0°C and -55°C should be taken as the same as that shown for 25°C. Typically these values are slightly better than those shown at 25°C.

The minimum time to toggle after the flip-flop has been set or reset is shown in Figure 9. Worst case data are: width of the set/reset pulse 6 ns minimum, width of the $\overline{K}/\overline{J}$ pulse 8 ns minimum, and the minimum spacing is 8 ns between the falling edge of the set/reset pulse and the rising edge of the $\overline{K}/\overline{J}$ pulse. Times are measured from the 50% portions of all waveforms.

Figure 10 illustrates the minimum required time to reset/set after a $\overline{J}/\overline{K}$ input has been received. This figure indicates the internal time constants of the flip-flop. Under worst case conditions the flip-flop will reset/set with a minimum pulse width of 10 ns, if the pulse is received 11 ns or more after the $\overline{J}/\overline{K}$ input. The worst case times are approximately 1 ns longer than the worst case propagation delay times (Figure 7).

If the $\overline{J}$-$\overline{K}$ inputs to a flip-flop are spaced far enough apart in time, they will act as set-reset inputs (all other inputs at a low level). While if they are brought close enough together, they will act as a toggle input to the flip-flop. Figure 11 illustrates the minimum required time to insure that the $\overline{K}$ input dominates after a $\overline{J}$ input. If the inputs are closer together (time-wise) than that shown for worst case, the flip-flop may toggle. Time to dominate may go as low as 2.0 ns at -55°C for some devices. Therefore, it is recommended that when it is desired to toggle a device, that the particular $\overline{J}$-$\overline{K}$ inputs be wired together rather than be fed through separate gates.

The "Power Dissipation vs. Temperature" curve (Figure 12) is primarily a measure of the device effective resistance over the temperature range. The worst case values are given for a single device, but values for worst case system design may be moved closer to the typical curve if desired. This is due to the averaging effect of multiple devices. Typically power dissipation changes less than 3 mW from D.C. to the maximum operating frequency of a given device. An unloaded flip-flop actually shows a decrease in power dissipation of about 2 mW from D.C. to above 70 MHz.

The sensitivity variation of a flip-flop (minimum input amplitude to toggle) vs. temperature is almost lost in measurement uncertainties. Typically, variations are well within ±10% which is insignificant in a system. Figure 13 illustrates that the typical device is more sensitive at -55°C than at 125°C. The sensitivity tracks very well with typical output amplitude vs. temperature which is shown in Figure 14.

The sensitivity of a flip-flop changes with supply voltage (V_{EE}) as does the output amplitude. Figures 15 and 16 illustrate the tracking capabilities of sensitivity and output amplitude vs. V_{EE}. It is seen that tracking is very good for ±30% variations in V_{EE}. The higher sensitivity at reduced V_{EE} suggests using the device as an RF amplifier, which also divides the input frequency by two. The effective gain through the flip-flop is typically greater than 2.5 at $V_{CC} = -4.0$ V.

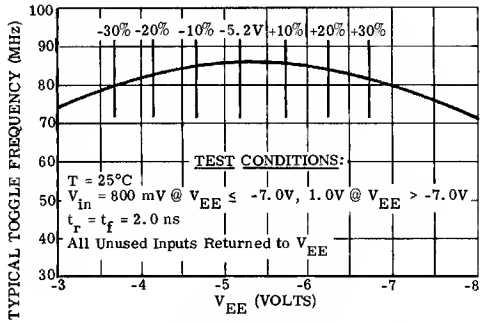


FIGURE 5 — TYPICAL TOGGLE FREQUENCY versus V_{EE}

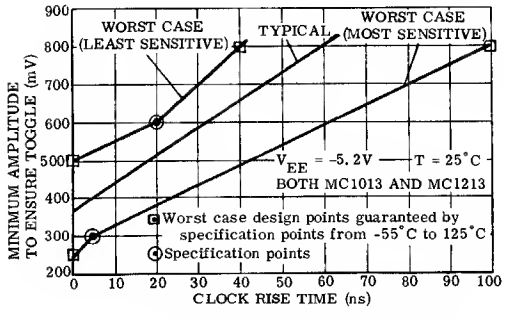
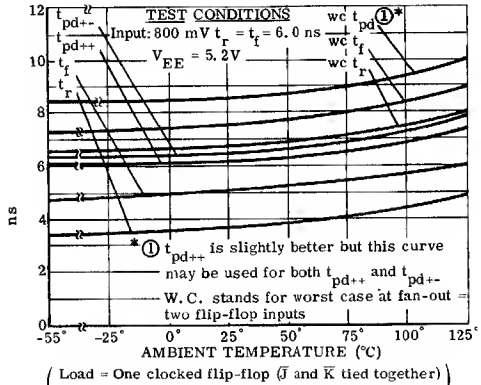


FIGURE 6 — AMPLITUDE versus RISE TIME TO INSURE TOGGLE

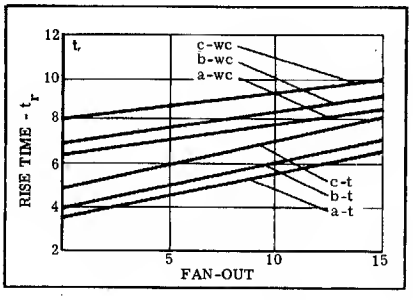
ADDITIONAL FLIP-FLOP CHARACTERISTICS

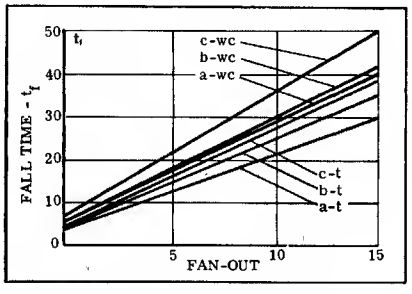
The flip-flop may be set and reset at a rate in excess of 100 MHz. The optimum pulses in this mode of operation are from 4 to 5 ns in width with rise and fall times of less than 2 ns. The MC1013/MC1213 flip-flop exhibits a tighter distribution of parameters than devices in the MC300/MC350 Series. 90% of the devices exhibit less than ±20% variations in propagation delay, rise, and fall times. Also, the maximum toggle frequency varies

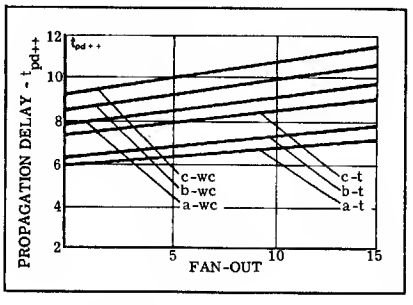


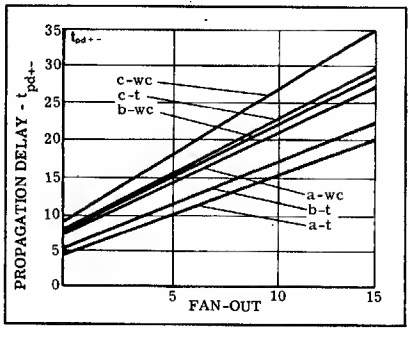
(Load = One clocked flip-flop ($\overline{J}$ and $\overline{K}$ tied together)
All unused inputs are returned to -5.2V)

FIGURE 7 — PROGAGATION DELAY TIMES, RISE TIME, FALL TIME versus TEMPERATURE









INPUT t_r = 5.0 ns — A = 25°C

INPUT AMPLITUDE 800 mV — B = 75°C

V_{EE} = -5.2V — C = 125°C

T = TYPICAL — WC = WORST CASE

FIGURE 8 — PROPAGATION DELAYS, RISE TIME, FALL TIME versus FAN-OUT AND TEMPERATURE

only about ±15% from the nominal value of 85 MHz. Each $\overline{J}$ and $\overline{K}$ input should be considered as a load of one, making a clocked input equivalent to a load of two. The maximum recommended fanout for the flip-flop is 15, above which, fall times become excessive. At low operating frequencies, fanout may be greatly increased if waveform deterioriation is considered in the design. The device has a guaranteed D.C. fanout of 25 which corresponds to a worst case of 2.5 mA load current. The maximum output current that should be drawn from the flip-flop is 10 mA which will decrease the nominal "1" level at no load by about 150 to 200 mV. If the flip-flop is used to drive a gate, the "1" level noise immunity is reduced to about 50 mV under these conditions. At large fanouts, fall time and t_{pd+-} will be decreased if an additional resistor is wired between the output and V_{EE}.

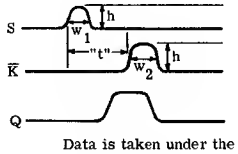
It should be noted that if a DC set or reset input is at a "1" level and the $\overline{J}$-$\overline{K}$ inputs are clocked, that a "glitch" will appear on the outputs. This glitch may be of sufficient amplitude to toggle or clock another flip-flop tied to the Q or $\overline{Q}$ output. This condition is the same as applying both a set and reset input to a current mode R-S flip-flop where both outputs tend to go to a V_{BB} level (half-way between "1" and "0"). This glitch may be minimized by a clock of low amplitude and slow rise time, but good system design eliminates this situation.

The worst case shift frequency depends upon the slowest flip-flop in the shift register. For a shift register without gating, the worst case shift frequency is essentially the same as the worst case toggle frequency of the slowest flip-flop employed in the register. Therefore, the worst case shift frequency is 70 MHz at 25°C and 55 MHz at 125°C.

This flip-flop is most useful in high frequency counters, phase locked loops, frequency synthesizers, special counters, logic designs that require additional $\overline{J}$ and $\overline{K}$ inputs, and high speed registers in the arithmetic portion of digital computers.

SUMMARY

The MC1013/MC1213 flip-flop is a versatile high frequency device that more than doubles the maximum operating frequency of a MECL system. The worst case data given in this note are conservative and, therefore, intended for system design. Due to the high frequencies of operation, performance depends heavily upon system layout. This MECL flip-flop will work best when used with multilayer printed circuit cards where lead lengths have been minimized. This flip-flop is characteristic of MECL II devices which operate in the 5 ns region with typical system loads.



w_1 = 4 ns (optimum)

w_2 = 6 ns (optimum)

h = 800 mV

Data is taken under the following conditions:

S and $\overline{K}$ inputs: $t_r = t_f$ = 1.5 ns

V_{EE} = -5.2V

t = min of 7-10 ns, "t" - w_1 = 3-6 ns min @ 25°C

Worst Case Operation -55°C to 125°C

w_1 = 6 ns min w_2 = 8 ns min "t"-w_1 = 8 ns min

FIGURE 9 — MINIMUM TIME TO TOGGLE AFTER SET DR RESET

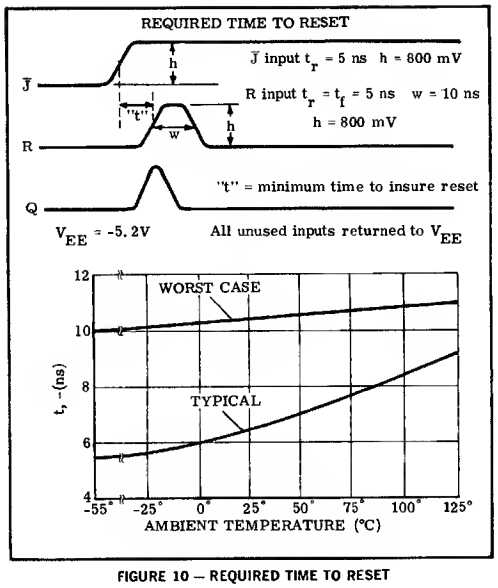


FIGURE 10 — REQUIRED TIME TO RESET

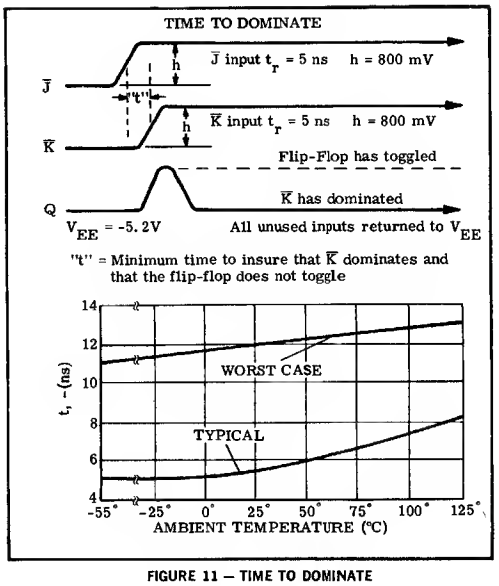


FIGURE 11 — TIME TO DOMINATE

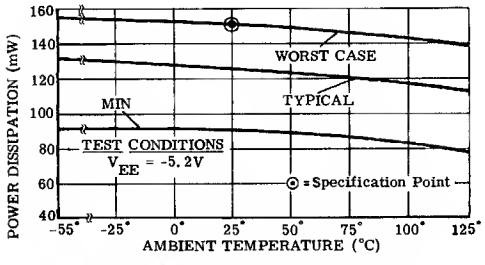


FIGURE 12 — POWER DISSIPATION versus TEMPERATURE

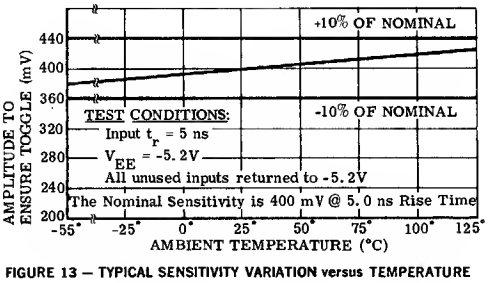


FIGURE 13 — TYPICAL SENSITIVITY VARIATION versus TEMPERATURE

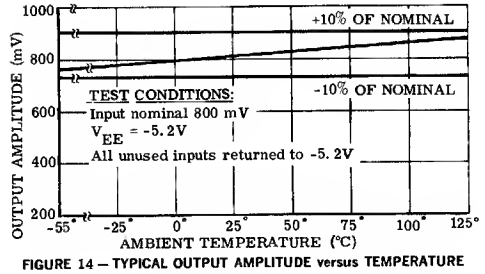


FIGURE 14 — TYPICAL OUTPUT AMPLITUDE versus TEMPERATURE

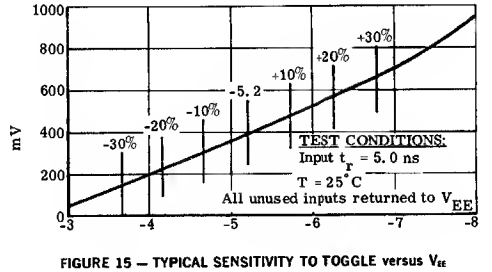


FIGURE 15 — TYPICAL SENSITIVITY TO TOGGLE versus V_{EE}

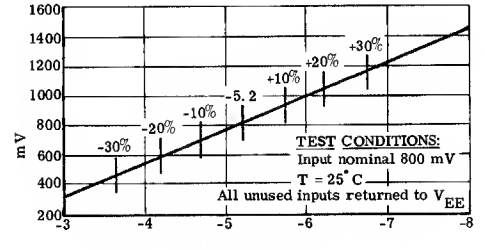


FIGURE 16 — TYPICAL OUTPUT AMPLITUDE versus V_{EE}

USING SHIFT REGISTERS AS PULSE DELAY NETWORKS

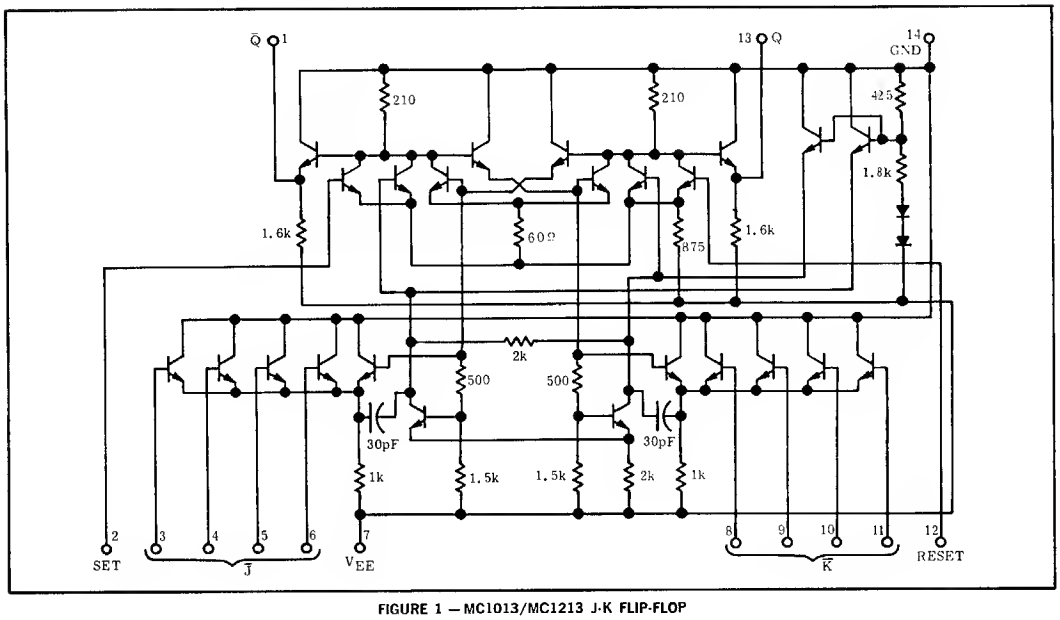
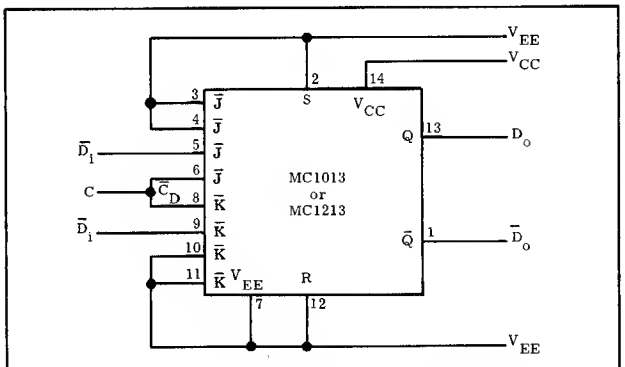


FIGURE 1 — MC1013/MC1213 J-K FLIP-FLOP



V_H = logical "1"
V_L = logical "0"

R	S	Q^{n+1}
0	0	Q^n
0	1	1
1	0	0
1	1	ND

Q^{n+1} = state of the flip-flop at time = t+1
ND = not defined

J̄	K̄	$\bar{C}_D$	Q^{n+1}
Ø	Ø	0	Q^n
0	0	1	$\bar{Q}^n$
0	1	1	1
1	0	1	0
1	1	1	Q^n

Note: pin 14 = Gnd = V_{CC}
pin 7 = -5.2V = V_{EE}
all unused inputs are returned to V_{EE}

A relatively high level voltage (-.75V) is defined as a logical "1" while a logical "0" corresponds to (-1.55V). The J̄ and K̄ inputs represent static logic levels while $\bar{C}_D$ refers to a dynamic logic swing. The J̄ or K̄ inputs should be changed to a logic "1" while $\bar{C}_D$ is at a high level; otherwise the J̄ or K̄ signal may clock the flip-flop. Ø = either logic 1 or 0 may be present.

FIGURE 2 — FLIP-FLOP LOGIC BLOCK, J̄-K̄ AND R-S TRUTH TABLES

INTRODUCTION

With the availability of flip-flops that will shift at rates in excess of 70 MHz, high speed shift registers are easily fabricated. These MECL II devices allow a shift register to be employed as a variable digital delay line in many applications. The pulse width degradation and delay errors are shown to amount to uncertainties of a maximum of one clock period for asynchronous inputs. This would amount to 20 ns for a 50 MHz shift register.

The flip-flop used in this application note is the MC1013 (0 to 75°C) or MC1213 (-55 to 125°C). The device is a J̄-K̄ type flip-flop with four J̄ and four K̄ logic inputs, one Reset input, one Set input, and Q-Q̄ outputs. The 70 MHz flip-flop is a member of the MECL II Multifunction family which is available in the dual in-line, 14 pin plastic package (0 to 75°C) and the 14 lead 1/4"×1/4" ceramic flat pack. Flip-flop specifications are: minimum toggle frequency = 70 MHz at 25°C; typical toggle frequency = 85 MHz. Oversensitivity (adequate noise immunity) — the device will not toggle at 5 ns rise time and less than 300 mV input. Adequate sensitivity — the device will toggle at 20 ns rise time and an input greater than 600 mV. The flip-flop will toggle on rise times of 40 ns or less at the nominal input amplitude of 800 mV. Worst case toggle and shift frequency is 55 MHz or better over the full temperature range, -55°C to +125°C. Operating voltage is -5.2 V with negligible degradations in characteristics for ±20% variations in supply voltage. Typically rise, fall, and propagation times are from 3.0 to 7.0 ns.

Figure 1 gives the schematic of the MC1013/MC1213 with nominal values of resistance. Circuit operation is the same as explained in AN244 for the MC314/MC364. The only differences are the extra $\overline{J}$ and $\overline{K}$ inputs and improved processing that decreases internal time constants.

Figure 2 illustrates a single flip-flop logic block connected as a single stage of a shift register. The $\overline{J}$-$\overline{K}$ and R-S truth tables are also shown in the figure. For shift register operation, the $\overline{J}$ and $\overline{K}$ inputs are always complements.

DELAY REGISTER OPERATION

Figure 3 is the logical schematic for an "n" bit shift register which includes the necessary logic for electronically controlling the delay of the register in powers of two. The incoming data to be delayed is considered to be asynchronous with the internal clock oscillator and random in nature. The input data (D_I) might appear as shown in Figure 4. The figure illustrates typical waveforms that would result from D_I and a 50 MHz clock.

G_1 is used to split the input into Data (D) and Data Not ($\overline{D}$) since the remaining logic requires complementary data (dual rail logic). The OR and NOR outputs of a gate have essentially the same propagation delay so output skew is no problem. G_2 and G_3 form a logic switch that "switches off" the input data whenever C is low ($\overline{C}$ high). This prevents the undesirable transfer of data into the first $\overline{J}$-$\overline{K}$ flip flop while the clock is at a low level. If the clock input to a $\overline{J}$-$\overline{K}$ flip flop is low, a positive going waveform on $\overline{J}$ would SET the flip flop to the "1" level (Q high) or a positive going waveform on $\overline{K}$ would RESET the flip flop (Q low). This feature is undesirable in this application.

Gates G_4 and G_5 form an R-S flip flop that stores the previous input data while $\overline{C}$ is at a high level. On the positive going transition of C, the data stored in G_4-G_5 is shifted into the first $\overline{J}$-$\overline{K}$ flip flop. The J-K is then inhibited by the high level of the clock. On the positive going edge of C, new data may be started through G_2 and G_3 into G_4-G_5. The input data is delayed through gates G_1 through G_5 and then an additional delay of τ (clock period) as it is shifted through each $\overline{J}$-$\overline{K}$ flip flop.

Figure 4 illustrates several of the possible timing conditions that may occur between D_I and the clock waveforms. For example, D_I is low between time 2.3 and 3.3. This is the longest low level on the input that will not be recognized by the shift register. From the timing diagram, it is seen that if an input is present for longer than the clock period, it will be recognized and shifted through the register. The low level data between 4 and 4.5 is present long enough to be recognized, and is stretched to one clock period in length by the input gating and flip flop #1. Also the positive pulse between time 12 and 12.5 is long enough and in the proper position to be recognized.

The input levels f_0-f_8, shown in the lower portion of Figure 3, allow the selection of the clock frequency $\frac{f}{2^m}$

where m is the number of the flip flops used to divide the basic frequency of the clock oscillator. Inputs f_0-f_8 are negative logic inputs, i.e. only one input should be low at a time. The low input will enable the desired clock frequency. If all inputs go high, the register will store the data that was being shifted in the register.

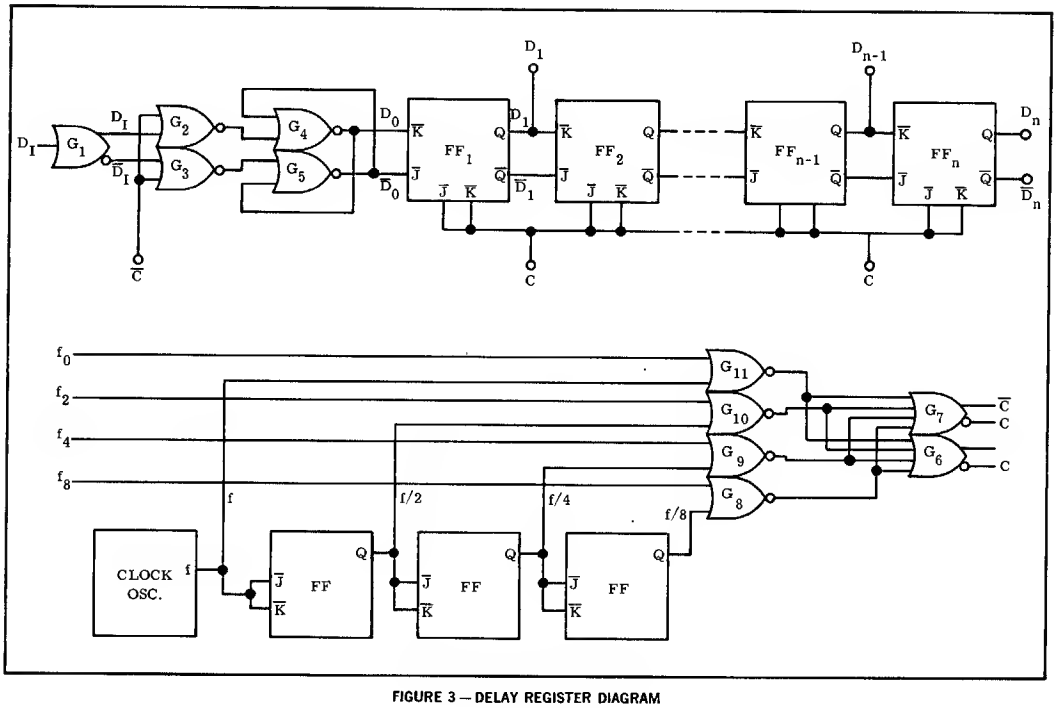


FIGURE 3 — DELAY REGISTER DIAGRAM

The preferred gate for G_1 through G_7 is the MC1023 which is a clock driver and high speed gate. This device exhibits typical propagation delays, rise, and fall times of 2ns. Two clock drivers are shown in Figure 3 where it is assumed that the number of stages in the register is ten or more. The MC1023 is a dual 4-input OR-NOR gate. By using both gates, 10 flip flops may be driven with a typical rise time of 2ns and fall time of 3.0ns. If lead lengths are kept short and low inductance printed circuit wiring employed, the register as shown in Figure 3 will shift at clock rates in excess of 70 MHz at room temperature.

Typically the delay through the input gating using the MC1023 is a minimum of 6ns or a maximum 6ns + $\frac{\tau}{2}$. This amounts to a minimum of 6ns and a maximum of 16ns for a 50 MHz clock, depending upon the relative position of the data and the clock. The delay from D_0 to D_1 is a minimum of $\frac{\tau}{2}$ plus the delay of flip flop 1 or a maximum of τ plus the flip flop delay. For 50 MHz operation, this yields a minimum of 15ns or a maximum of 25ns. The total delay from D_I to D_1 is then a minimum of 21ns or a maximum of 41ns. The incremental delay from flip flop 1 to flip flop 2 is τ and so forth throughout the delay register.

Assuming a 50% duty cycle clock, delay uncertainty of input information is $\pm \frac{\tau}{2}$ and the maximum length of an input datum that may not be recognized is τ. Also an input datum may be lengthened or shortened by as much as τ. The delay of the register shown, using the recommended devices is approximately 11ns + $n\tau \pm \frac{\tau}{2}$, where n is the number of MC1013/MC1213 J-K flip flops between the input and desired output, and τ is the period of the clock waveform.

Further improvement in delay register characteristics may be obtained by using the MC1022 "D" type flip flop. The input is single rail, eliminating the need for G_1. Since the flip flop operates on the master slave principle, gates G_2 through G_5 may also be eliminated. The data input is then brought directly into the flip flop with no additional gating. The delay through a register using the MC1022 is approximately 5ns + $n\tau \pm \frac{\tau}{2}$ where n is the number of "D" flip flops used including the first stage. Typically the "D" type flip flop will operate at greater than 60 MHz allowing values of τ as small as 16.5 ns.

SUMMARY

The MC1013/MC1213 may be used in shift register applications at speeds greater than 50 MHz over the specified temperature range. Incremental delays of 20ns are easily obtained and continuously variable delays are possible with variable clock frequency.

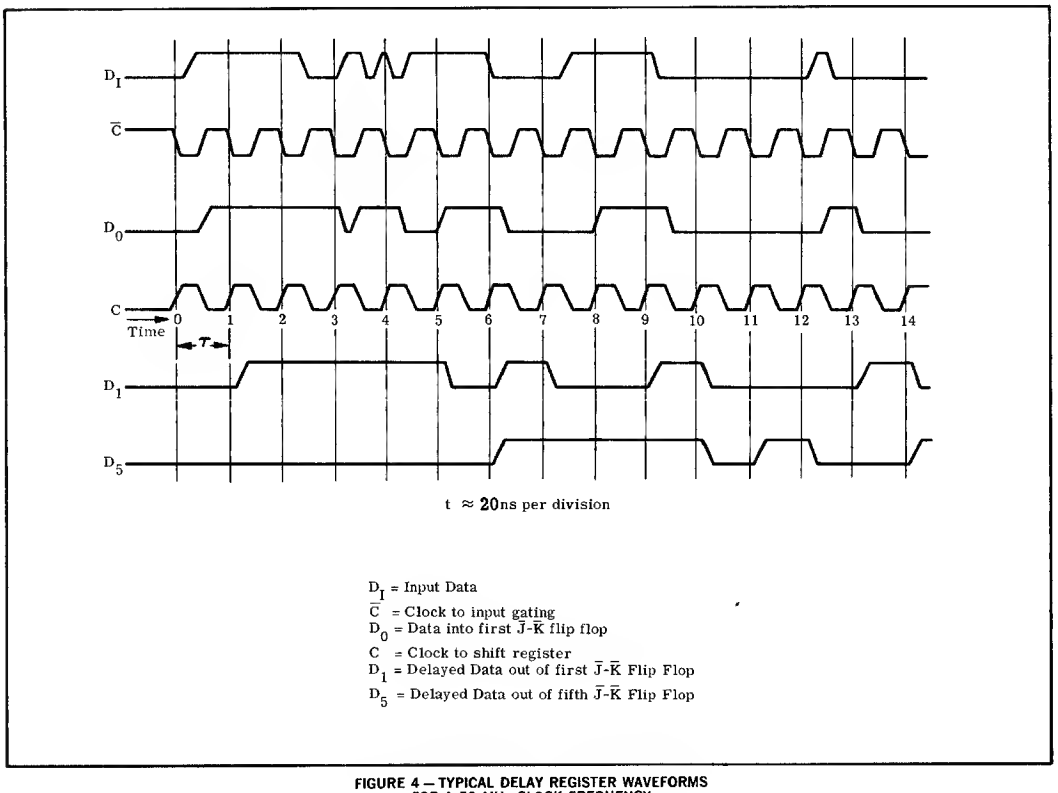


FIGURE 4 — TYPICAL DELAY REGISTER WAVEFORMS FOR A 50 MHz CLOCK FREQUENCY

OVERSHOOT AND RINGING IN HIGH SPEED DIGITAL SYSTEMS

Whenever a switching circuit with low output impedance and fast risetime is used to drive a signal lead that is connected to several gates, overshoot will be present. The term overshoot, as used in this note, is defined as the peak to peak voltage difference between the most positive portion of the rising edge of a waveform and the "1" logic level of the waveform after all transients have decayed. In general, the lower the output impedance of a gate, the faster the risetime, the longer the wiring length, and the larger the fanout, the greater the overshoot caused when switching occurs. This note contains several tables and sets of photographs illustrating the overshoot that can be expected under various worst case configurations and loadings. Methods of overshoot reduction are applied with tabulated results from which general conclusions and guidelines are drawn.

The exact simulation of an integrated circuit load or the loading of several devices is extremely difficult with passive components. This is due to the complex and non-linear input impedance of a MECL device. The input capacitance goes through a peak value of approximately 15pF during a logic transition and averages out to less than 5pF over the entire logic swing. The input resistance will be about 50KΩ (worst case) at a logic "1" level. The input resistance will decrease exponentially if saturation of the MECL input is approached. (A MECL gate may be driven into saturation by sufficient overshoot on the input waveform, especially at high temperatures.) For system design purposes a worst case input capacitance of 5pF per device input and a 50k resistance to V_{EE} may be utilized. If sockets for the gates are used, an additional 1pF should be added per gate input. Wiring capacitance using teflon coated wire is about 1 pF per inch. Inductance per unit length of wire is about 0.02 μH per inch. These values will vary by a large amount depending upon "lead dress" and, therefore, should be considered only as "ball park" figures. When circuit measurements are being made, oscilloscope probe capacitance should be considered. The capacitance of a probe will vary from 1.8pF to about 10pF depending upon the probe design.

Attempts were made to simulate the loading caused by various fan-outs with discrete components. The best simulation was obtained by the following circuit, Figure 1, which will help to explain the parameters affecting overshoot. R_O stands for the output incremental resistance of the gate used as a driver. Values are approximately: MC301--20Ω, MC365--12Ω, MC369--5Ω. L is the series inductance of the signal lead and R_I is the input resistance of the gates used as the load. C is the shunt capacitance caused by the fan-out, wiring capacitance, socket capacitance, and probe capacitance. The value of C is 8-10pF per fan-out. R_D is necessary to damp out excessive overshoot which is caused by the lumped value of C. C is chosen to give rise time equivalent to the measured value for the given fan-out. R_D is on the order of 20Ω with higher values for small fan-out and smaller values for large fan-outs.

This load only simulates overshoot and rise time as can be seen by comparing photographs 2, 8, and 14 with 5, 11, and 17 respectively. The period of oscillation is longer for the simulated load, indicating that the value of C is higher than with the actual load. The effective capacitance of the actual load may be shown to be about 6-7pF per fan-out, i.e. 2-3pF less than in the simulated load. The difference in period of oscillation and damping indicates just how approximate the simulated load is.

How much overshoot can occur under worst case conditions in a MECL system? This question is answered by the data which are shown in the following tables. These data were obtained by using the MC301, MC365, and MC369 gates as drivers. MC356's and MC364's were used as fan-out devices. Lead lengths of 3", 6" and 12" were used with the loads constructed on printed circuit boards and plugged into a single socket which terminated the particular lead. This simulates a worst case situation since fan-out is not usually lumped at the end of a single lead. The devices used as drivers were picked at random and other devices may give somewhat different results due to output impedance and output risetime.

How much overshoot can be tolerated in a MECL system? This question is relatively easy to answer in the case of driving flip-flops, but becomes more difficult when referring to gates. When driving flip-flops, one $\bar{J}$ input may be clocked and the other inhibited at a worst case "1" level. If the level of the clocked J input exceeds the inhibiting level on the other J input by more than the required amplitude to toggle a sensitive flip-flop, then false information may be passed into the flip-flop. For room temperature operation, overshoot should

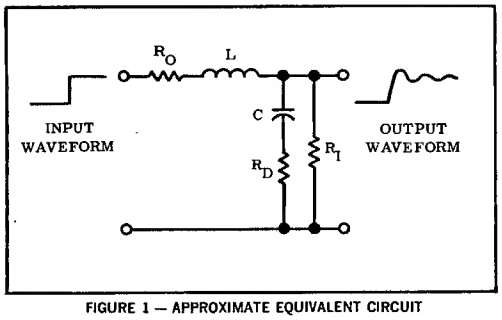


FIGURE 1 — APPROXIMATE EQUIVALENT CIRCUIT

DRIVER GATE	FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	2-MC356	5mV	8.9ns	10mV	7.7ns	50mV	6.8ns
MC301	5-MC356	40mV	9.2ns	60mV	8.5ns	110mV	8.0ns
MC301	10-MC356	90mV	10.9ns	115mV	10.9ns	175mV	11.1ns
MC301	15-MC356	95mV	12.1ns	135mV	12.0ns	200mV	12.3ns
MC365	2-MC356	40mV	6.7ns	70mV	6.2ns	145mV	5.4ns
MC365	5-MC356	80mV	6.9ns	140mV	6.6ns	215mV	6.6ns
MC365	10-MC356	150mV	8.2ns	205mV	8.2ns	270mV	8.4ns
MC365	15-MC356	180mV	9.0ns	220mV	10.0ns	300mV	10.3ns
MC369	2-MC356	80mV	4.2ns	200mV	4.5ns	300mV	4.4ns
MC369	5-MC356	120mV	5.2ns	220mV	5.5ns	330mV	6.3ns
MC369	10-MC356	160mV	7.4ns	220mV	7.7ns	350mV	9.1ns
MC369	15-MC356	200mV	8.9ns	270mV	9.0ns	370mV	9.9ns

TABLE 1 — MEASURED OVERSHOOT AND RISE TIME MC3S6 AS LOAD

ORIVER GATE	J-K COMMON FAN-OUT	3" LEAD LENGTH		6" LEAD LENGTH		12" LEAD LENGTH	
		OS	RT	OS	RT	OS	RT
MC301	1-MC364	0mV	7.5ns	0mV	7.8ns	0mV	6.0ns
MC301	2-MC364	45mV	7.5ns	70mV	7.3ns	135mV	7.2ns
MC301	5-MC364	85mV	8.6ns	130mV	8.8ns	200mV	8.8ns
MC301	10-MC364	160mV	12.8ns	190mV	13.0ns	270mV	13.5ns
MC365	1-MC364	0mV	6.7ns	0mV	4.7ns	55mV	4.8ns
MC365	2-MC364	100mV	5.9ns	165mV	5.8ns	250mV	6.0ns
MC385	5-MC364	160mV	6.7ns	210mV	6.9ns	340mV	7.3ns
MC365	10-MC384	180mV	9.9ns	230mV	11.3ns	370mV	11.5ns
MC369	1-MC364	0mV	4.5ns	50mV	4.1ns	280mV	4.1ns
MC369	2-MC364	180mV	4.9ns	280mV	5.0ns	350mV	5.4ns
MC369	5-MC364	250mV	6.0ns	340mV	6.4ns	420mV	6.4ns
MC369	10-MC364	250mV	6.8ns	340mV	8.3ns	440mV	10.1ns

TABLE 2 — MEASURED OVERSHOOT ANO RISE TIME MC364 (CLOCKEO) AS LOAD

LOADING		MAXIMUM SERIES RESISTANCE (R_S)		
OC FAN-OUT	MAXIMUM EQUIVALENT LOAD CURRENT	STANDARO GATE DRIVER R_O=22	LINE DRIVER MC315/MC365 R_O=15	CLOCK ORIVER MC368 R_O=5
25	2.5mA	0	7	17
15	1.5mA	14	21	31
10	1.0mA	33	40	50
5	0.5mA	88	95	105
3	0.3mA	160	170	180
2	0.2mA	250	260	270
1	0.1mA	530	535	545

NOTE: Worst Case values are calculated from $R_O + R_S = \frac{\Delta V}{\Delta I}$

ΔV = 55mV maximum allowed "1" level voltage change (no load to full load)

ΔI = change in load current (no load to full load) for given fan-out

R_O = incremental output resistance of driver gate

R_S = series resistance added in lead between driver and fan-out

TABLE 3 — MAXIMUM ALLOWED VALUES OF SERIES RESISTANCE VS. FAN-OUT

be less than 150 mV. For worst case design over the full temperature range (-55°C to +125°C), overshoot should be limited to 100 mV or less. Although a regular gate will tolerate far more overshoot than the above-mentioned values, the worst case value of 100 mV should be used in system design. If high overshoot levels occur in a system, problems caused by the cross-coupling of noise from one signal lead to another will be compounded. For example, if 200 mV of overshoot is allowed, a normal transition of 800 mV would be changed to a 1V transition, therefore increasing cross-coupling of noise by 25%.

It is obvious that the worst case values of overshoot shown in Tables 1 and 2 are excessive. How then can overshoot be reduced? It can be seen from the approximate equivalent circuit, Figure 1, that overshoot and the associated ringing is caused primarily by the values of L and C which dominate the other parameters for large fan-outs. Overshoot may be reduced by decreasing L and C and/or adding to the damping by increasing R_O or R_D. The value of L may be decreased by running the lead close to a ground plane or using a flat conductor that has less inductance per unit length. Figures 3, 9, and 15 compared with 4, 10, and 16 respectively, show the striking difference in overshoot for 12" of teflon coated wire driving a fan-out of 15 gates when the wire is touching the ground plane and when it is an average of 3" above the ground plane. The value of C is difficult to reduce. The equivalent capacitance per gate input may be varied by perhaps 2pF depending upon the use of sockets or the direct wiring of the integrated circuits, and the method of wiring used.

The most effective method of reducing overshoot is the reduction of $L\frac{di}{dt}$, the voltage drop across L due to the rate of change of current. One way to accomplish this is by decreasing lead length or running multiple wires between the driver and load. This method is often not practical. The insertion of a resistor in series with the lead, thus increasing the series damping resistance, is the most effective method of overshoot reduction. The time constant of the transmission path is then increased, therefore causing a trade-off with risetime. The addition of a resistor causes a DC voltage drop and large values must be avoided to prevent "1" level degradation. Table 3 gives the maximum value of series resistance that may be inserted for worst case design for a given fan-out and driver.

Since capacitively coupled flip-flops toggle on peak-to-peak amplitude and are relatively unaffected by voltage input levels, higher values of series resistance may be employed. The limit on the values of resistance is determined by the worst case amplitude vs. risetime curves which may be found in AN244. The added resistance, if relatively large in value, forms an R-C integration network which determines the risetime. This may be observed in Table 4.

It is seen from Table 4 that the values of required series resistance become marginal for high fan-outs with 12" signal leads when compared to the allowed values shown in Table 3. Therefore, when driving a high fan-out with fast risetime it may be more desirable to use the following method: A separate signal lead and series resistor from the driver to each fan-out is utilized. This method may be used for a fan-out of 20 clocked flip-flops using the MC369 as a driver. The risetime to each flip-flop or gate is appreciably less for this method than when driving the devices with a single signal lead and resistor.

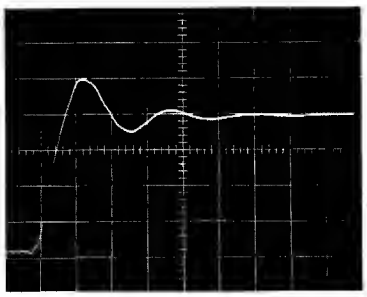
Another method of reducing overshoot is the addition of a ferrite bead around the signal lead between the driver and the load. This is another method of trading overshoot for risetime. Advantages of the ferrite bead are low cost and no shift produced in DC levels. Disadvantages are that it is effective for only small fan-outs, fast risetimes, and long lead lengths. The ferrite bead adds inductance to the signal lead at low frequencies, but this is an inductance of very low Q at high frequencies. Therefore, attenuation is produced for the high frequency components of the risetime, resulting in a slower risetime as seen by the load. Once the risetime is reduced to about 12ns, the addition of further ferrite beads to the signal line will not appreciably reduce overshoot and may actually increase overshoot for slower risetimes.

The following photographs will serve to illustrate the data shown previously. All photographs are taken with the following constants: Horizontal deflection rate 1cm per 20ns, Vertical deflection 1cm per 200mV, and signal lead lengths of 12 inches. The following notation is used for the photographs. OS = overshoot, tr = risetime, and W = 1/8", W = 0", W = 3" which stand for wire 1/8" above ground plane, 0" above ground plane and 3" above ground plane respectively. L stands for load with "A" being the actual integrated load and "S" being the simulated load. R_S is the value of series resistance inserted in the signal lead. The simulated load used in Figures 5, 7, 11, 13 was C = 150pF, R_D = 15Ω, R_I = 3K (refer to Figure 1), while the simulated load in Figures 17, 19 was C = 160pF, R_D = 8 , R_I = 3K.

DRIVER GATE	FAN-OUT	R	3" LEAD LENGTH OVERSHOOT	3" LEAD LENGTH RISETIME	R	6" LEAD LENGTH OVERSHOOT	6" LEAD LENGTH RISETIME	R	12" LEAD LENGTH OVERSHOOT	12" LEAD LENGTH RISETIME
MC301	10-MC356	0	90mV	10.9ns	5	100mV	11.7ns	18	95mV	12.8ns
MC301	15-MC356	0	95mV	12.1ns	12	90mV	14.3ns	12	95mV	14.4ns
MC301	5-MC364	0	85mV	8.6ns	13	90mV	9.9ns	27	100mV	10.2ns
MC301	10-MC364	10	95mV	14.2ns	13	100mV	14.6ns	24	95mV	15.9ns
MC365	10-MC356	10	90mV	9.4ns	15	95mV	9.8ns	25	95mV	10.3ns
MC365	15-MC356	10	100mV	10.3ns	15	100mV	10.9ns	24	95mV	11.8ns
MC365	5-MC364	20	95mV	8.5ns	27	100mV	8.7ns	51	90mV	9.8ns
MC365	10-MC364	13	95mV	11.9ns	18	95mV	12.6ns	27	95mV	13.8ns
MC369	2-MC356	0	80mV	5.1ns	24	90mV	5.4ns	62	100mV	6.0ns
MC369	5-MC356	5	100mV	5.9ns	24	100mV	6.8ns	43	100mV	7.6ns
MC369	10-MC356	10	100mV	8.7ns	24	90mV	10.5ns	33	90mV	11.4ns
MC369	15-MC356	10	95mV	10.2ns	18	95mV	11.4ns	27	95mV	12.7ns
MC369	1-MC364	0	0	4.8ns	0	50mV	3.9ns	68	90mV	4.0ns
MC369	2-MC364	27	100mV	5.9ns	62	95mV	6.7ns	75	100mV	6.8ns
MC369	5-MC364	22	90mV	7.5ns	39	100mV	8.2ns	47	100mV	8.6ns
MC369	10-MC364	15	90mV	10.9ns	22	100mV	11.9ns	33	100mV	13.4ns

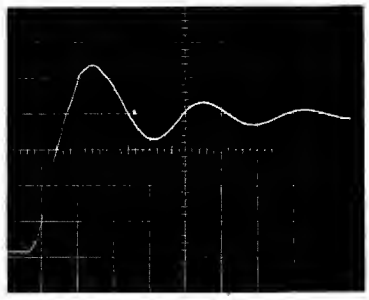
TABLE 4 — REQUIRED SERIES RESISTANCE TO REDUCE OVERSHOOT TO AN ACCEPTABLE LEVEL

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC301
FAN-OUT = 15 MC356'S



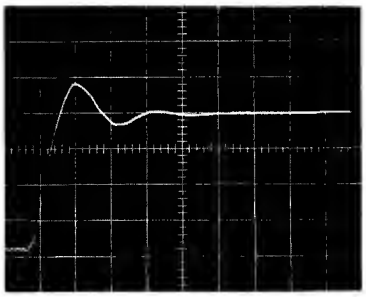
t_r = 12.3ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = A

FIGURE 2



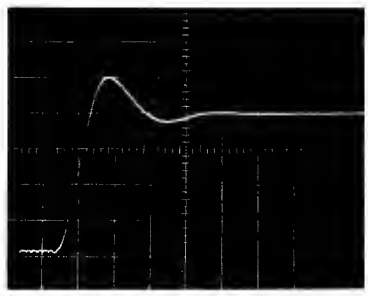
t_r = 14.2ns
w = 3"
R_S = 0Ω
OS = 280mV
L = A

FIGURE 3



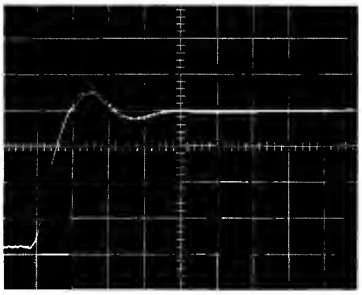
t_r = 12.3ns
w = 0"
R_S = 0Ω
OS = 175mV
L = A

FIGURE 4



t_r = 12.8ns
w = 1/8"
R_S = 0Ω
OS = 200mV
L = S

FIGURE 5



t_r = 14.7ns
w = 1/8"
R_S = 15Ω
OS = 95mV
L = A

FIGURE 6

t_r = 15.3ns
w = 1/8"
R_S = 15Ω
OS = 100mV
L = S

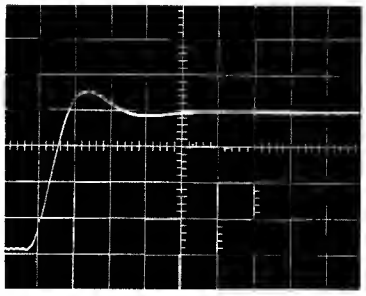
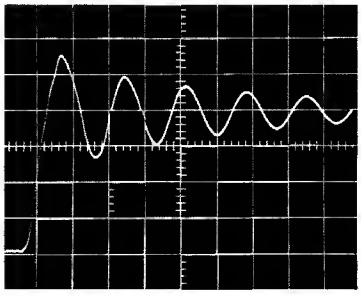


FIGURE 7

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC365
FAN-OUT = 15 MC356'S



t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = A

FIGURE 8

t_r = 12.9ns
w = 3"
R_S = 0
OS = 360mV
L = A

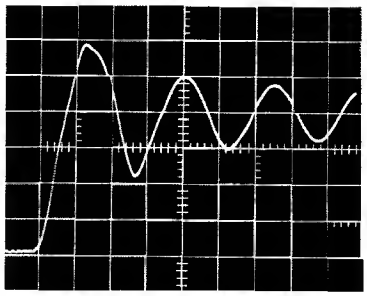
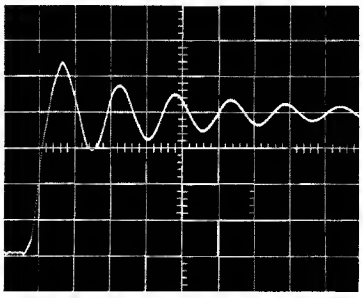


FIGURE 9



t_r = 9.5ns
w = 0"
R_S = 0
OS = 280mV
L = A

FIGURE 10

t_r = 10.2ns
w = 1/8"
R_S = 0
OS = 300mV
L = S

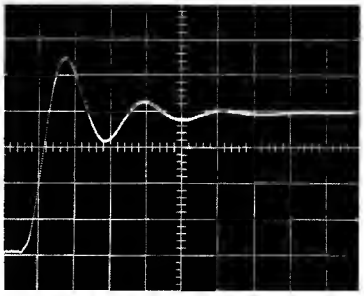
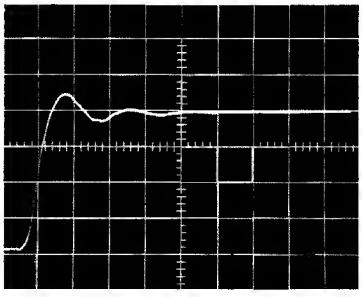


FIGURE 11



t_r = 11.8ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = A

FIGURE 12

t_r = 13.0ns
w = 1/8"
R_S = 24Ω
OS = 100mV
L = S

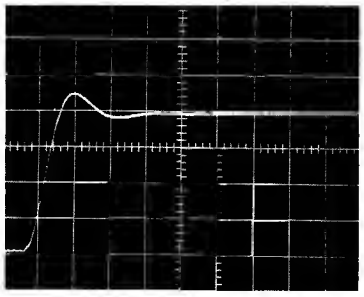
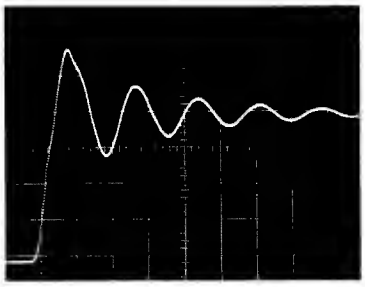


FIGURE 13

THE FOLLOWING SIX PHOTOGRAPHS ARE FOR DRIVER = MC369
FAN-OUT = 15 MC356'S



t_r = 8.8ns
w = 1/8"
R_S = 0
OS = 370mV
L = A

FIGURE 14

t_r = 12.0ns
w = 3"
R_S = 0
OS = 390mV
L = A

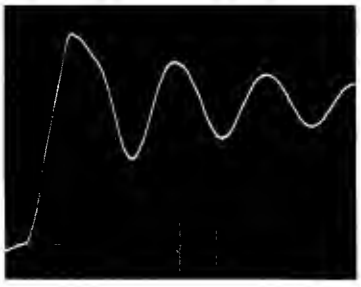
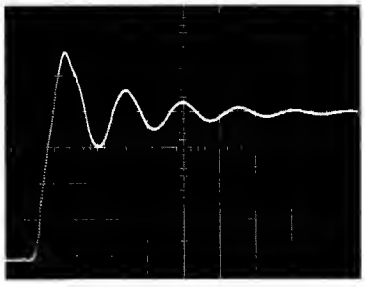


FIGURE 15



t_r = 8.3ns
w = 0"
R_S = 0
OS = 360mV
L = A

FIGURE 16

t_r = 9.2ns
w = 1/8"
R_S = 0
OS = 380mV
L = S

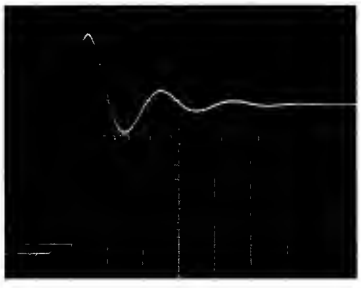
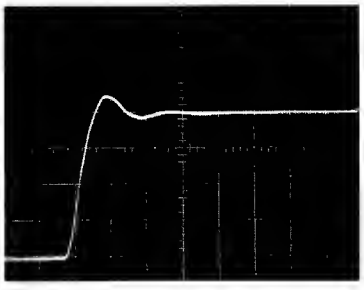


FIGURE 17



t_r = 11.6ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = A

FIGURE 18

t_r = 13.4ns
w = 1/8"
R_S = 27Ω
OS = 100mV
L = S

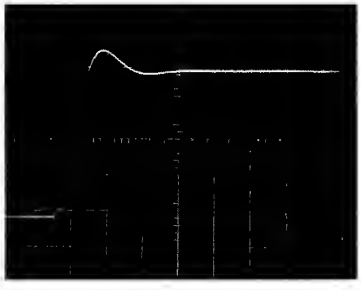


FIGURE 19

CONCLUSIONS

It has been shown that overshoot can be a system problem for long lead lengths and "lumped" fan-outs and that the amount of overshoot is primarily determined by system layout and geometries. Overshoot to typical fan-outs may be reduced to acceptable levels by inserting resistance of the proper value in series with the driver output lead. Higher fan-outs may be driven with fast risetimes by inserting a resistor of appropriate value in series with the input to each integrated circuit load, and running a separate lead from the driver to each resistor. Also, ferrite beads may be used to advantage for certain configurations of long leads and relatively low fan-outs.

As system speeds increase and MECL gates with risetimes of 2ns or less are utilized, these methods will not be useful for reducing overshoot. Strip line techniques utilizing multi-layer printed circuit boards, controlled line impedance, and terminated transmission lines will solve overshoot problems for logic into the sub-nanosecond region.

NOISE IMMUNITY WITH HIGH THRESHOLD LOGIC

INTRODUCTION

The following material discusses general noise considerations and compares the noise immunity of the new high threshold devices with standard saturated logic devices. Some basic illustrations are provided which indicate the flexibility of usage that may be achieved with the MHTL family.

Typical characteristics of the MHTL family are:

Single 15-volt power supply
7.5V switching threshold
6 volt signal line noise margins
13 volt logic swing
30 mW gate power dissipation
85 ns gate propagation delay
4 MHz flip flop toggle frequency
-30^{o} to $+75^{o}C$ operating temperature range

NOISE INJECTION

Electrical noise has always been a source of trouble for electronic systems whether they are composed of discrete components or integrated circuits. Origination of electrical noise can be from many sources both external to the electronic system under consideration and self-induced noise by the circuitry itself. Examples of external sources would be switching of inductive circuits, rotating machinery, and various electronic control circuits as depicted in Figure 1.

Internal noise may be caused by the switching of one circuit affecting the state of another circuit (Figure 2). The amount of noise induced into the passive circuit is a function of the voltage swing, current change, and the switching speed of the active circuit and the inductive and capacitive coupling between the two circuits. Coupling may also take place by the use of a common path for the active and passive devices such as a power supply or ground lead. Noise from external sources is induced into the system under similar conditions. Generally, noise is a random combination of many sources and as such is extremely hard to analyze. The net result, however, is that induced positive and negative spikes relative to the quiescent condition of a line may cause erroneous information to be absorbed into the system. This condition must be avoided if proper operation is to be achieved by the unit.

NOISE REDUCTION TECHNIQUES

Several schemes have commonly been employed to reduce the effect of electrical noise on a system composed of integrated circuits. Physical shielding of the integrated circuits and its associated wiring prevents external electromagnetic radiation from inducing noise into the circuitry. Special buffering circuits may be employed between the electronic circuits and signal leads dependent on external sources. These signal leads in many cases require special routing considerations and special shielding. Extra filtering of the power supply leads may be required to reduce the noise introduced by this route. Internal noise generation may require special spacing and routing considerations as well as maintaining short lead lengths. In some cases the power supply may need to be by-passed at several points on a board.

The amount of additional components and equipment necessary to protect integrated circuits from electrical noise can increase to a point where it is economically desirable to seek other methods of operation to obtain the desired results. It would be advantageous to have an integrated circuit family with a high degree of inherent noise immunity for economical construction of an electronic system. This will minimize the amount of special care needed for proper circuit operation in areas with a high electrical noise environment.

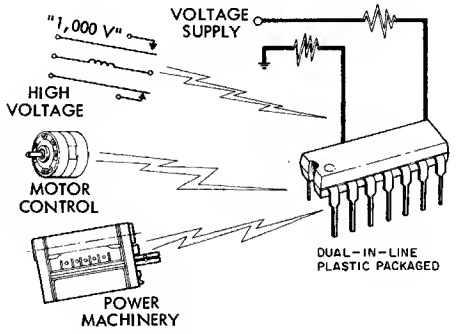


FIGURE 1 - EXTERNAL NOISE GENERATOR

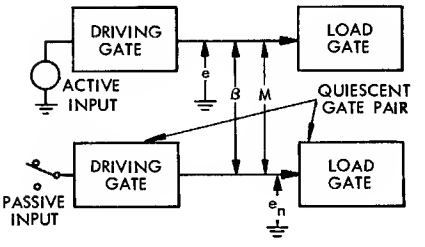


FIGURE 2 - INTERNAL NOISE GENERATOR

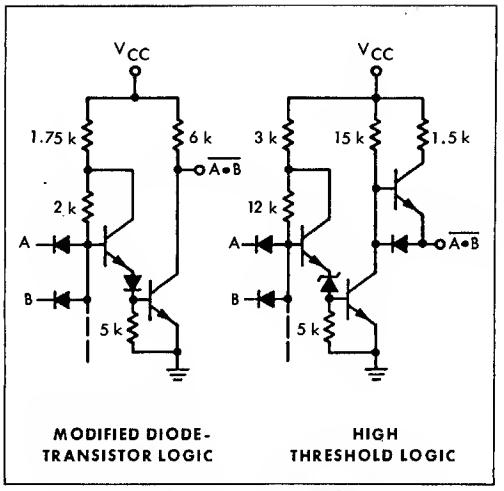


FIGURE 3 - GATE COMPARISONS

devices demands a higher power supply and a nominal 15 volts is used. The transfer curve for the basic gate operating with a 15 volt supply is shown in Figure 4. It can be seen that for any input signal up to 6.5 volts, the output will remain in the high state or above 13.5 volts. A 2-volt margin, from 6.5 volts to 8.5 volts, is used for the transition region and guards against variations between manufacturing lots and temperature effects from -30°C to +75°C. At 8.5 volts on the input, the output is in the low state or less than 1.5 volts and remains there for any further increase of the input voltage. This diagram indicates worst case noise margins of 5 volts in both the high and low states for a V_{CC} of 15 volts while typical values are about 6 volts.

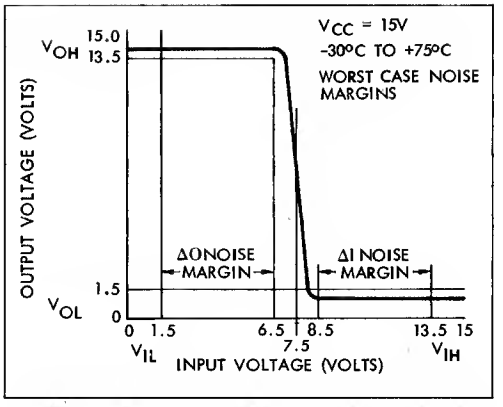


FIGURE 4 - TYPICAL HIGH THRESHOLD TRANSFER CURVE

LOGIC FAMILY COMPARISONS

BASIC OPERATING CHARACTERISTICS

A comparison of basic operating characteristics for high threshold logic with the standard forms of logic is provided in the table shown in Figure 5. The values given are typical for an ambient temperature of 25°C and indicate relative characteristics between the different families. One difference that should be noted is that the high threshold logic is slower than the other families. This characteristic aids in the rejection of noise and will be illustrated in following figures.

	V_{CC} (VOLTS)	GATE POWER DISSIPATION (mW)	PROPAGATION DELAY (ns)	DC NOISE IMMUNITY (VOLTS)	LOGIC SWING (VOLTS)
RESISTOR TRANSISTOR LOGIC	3.6	12	25	0.5	1.0
MODIFIED DIODE TRANSISTOR LOGIC	5.0	8	30	1.2	4.5
TRANSISTOR – TRANSISTOR LOGIC	5.0	15	10	1.2	3.5
HIGH THRESHOLD LOGIC	15	30	85	6	13

FIGURE 5 - BASIC OPERATING CHARACTERISTICS

A HIGH THRESHOLD LOGIC

The most popular families of integrated circuits in use today exhibit a comparatively high speed of operation and have typical threshold values between 0.7 and 1.5 volts. A new type of logic family, High Threshold Logic (MHTL), has been developed that closely resembles the modified diode-transistor logic family (Figure 3). The basic difference is that the high threshold logic uses a reverse biased base-emitter junction operating in the avalanche breakdown mode as a threshold element. As can be seen in the figure, the logical NAND function is provided by each gate. The inputs of the modified diode-transistor gate must exceed two forward base emitter drops or typically 1.5 volts before base current is applied to the output inverting transistor providing the "0" state. In the high threshold device, however, the inputs must exceed the reverse biased base-emitter breakdown plus one forward V_{BE} drop or typically 7.5 volts before the output inverting transistor turns on. Since the other logic families exhibit a threshold level similar to or less than the modified diode-transistor device, a considerable increase in threshold level has been obtained with the new configuration. The higher threshold incorporated in the

SIGNAL LINE NOISE IMMUNITY

Measurements were made on the different logic families to determine the signal line noise immunity not only from a voltage margin consideration, but also from a pulse width and energy point of view as well. Figure 6-A illustrates a test set-up to measure immunity of the gate to noise on the signal lead. Positive going noise was injected on the signal lead for this set-up with the output of gate #1 in the low state. When sufficient noise was injected, the flip-flop driven by the second gate would begin to toggle indicating the effect of the injected noise. This type of test not only measures the power needed for disturbance, but also the pulse width of noise necessary to propagate through and cause faulty operation of a driven device. A series of values of voltage level and injected current to cause disturbance were taken versus the pulse width at each corresponding point. Current readings were obtained as a voltage drop across the pulse generator resistor. The pulse generator offset voltage was adjusted to eliminate the effect of its quiescent condition on gate levels. Voltage threshold as a function of pulse width is plotted in Figure 6-B. The energy of each logic family is plotted in bar graph form at the knee of each respect-

ive curve in Figure 6-C. For narrower pulse widths, the energy necessary to cause a disturbance increases. The high energy value obtained for MHTL is a result of the high threshold voltage and low gate impedance in this state.

Figure 7-A illustrates a similar test except that gate #1 is in the high state and negative going noise is injected on the signal lead. Similar results are shown in Figure 7-B and C.

GROUND LINE IMMUNITY

Tests were made on the devices to provide information on the immunity to noise injected on the ground terminal. The test configuration is shown in the first part of Figure 8. A plot of voltage threshold versus pulse width is given in Figure 8-B for the worst case condition found for the particular family dependent on the input state. The energy relationships are provided in Figure 8-C.

POWER SUPPLY IMMUNITY

A similar test was made for noise injected on the power supply lead. In this case, the flip flop will only be affected by negative going noise and the results indicate worst case conditions for the particular family dependent on the state of the first gate. The test configuration and results are given in Figure 9.

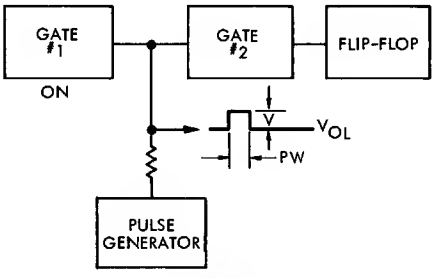


FIGURE 6A

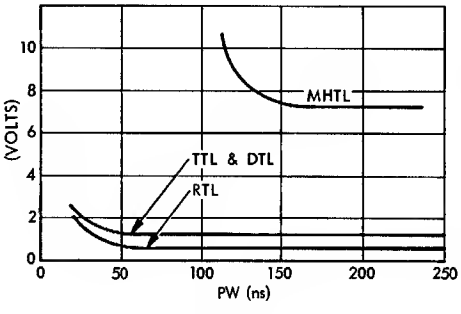


FIGURE 6B

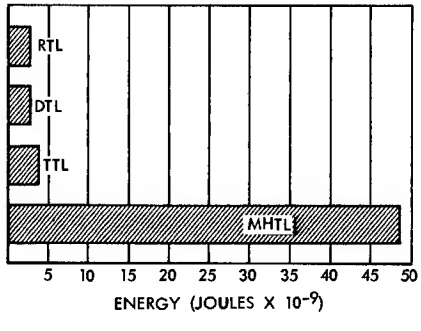


FIGURE 6C

SIGNAL LINE NOISE IMMUNITY

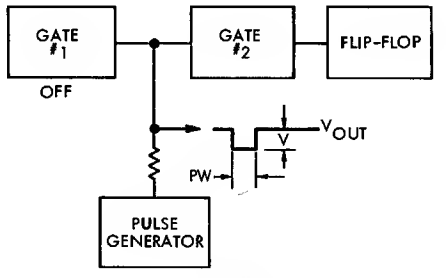


FIGURE 7A

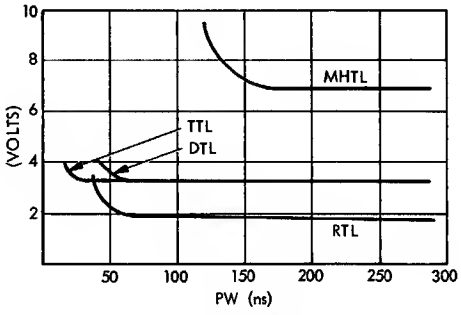


FIGURE 7B

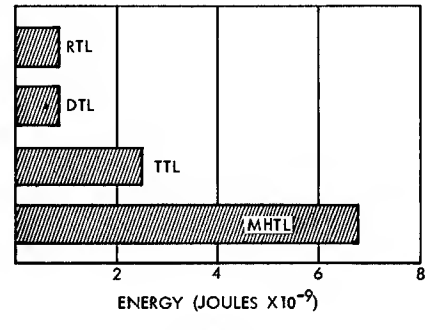


FIGURE 7C

SIGNAL LINE NOISE IMMUNITY

The preceding tests were taken with a fanout of one on the first gate and a fanout of the flip flop only on the second gate. This condition tends to be an advantage for the RTL family and the results are somewhat optimistic in this case.

These comparisons indicate that the high threshold logic has an appreciable inherent advantage over the standard families of integrated circuits. In addition, the higher threshold level present in these devices provides a considerable margin that may be used in conjunction with simplified buffering networks to filter out excessive noise spikes under very extreme conditions.

USAGE

The preceding discussion has generally referred to the basic high threshold gate circuit. Additional components are available, however, which exhibit the same noise immunity characteristics obtained by reverse biased base-emitter breakdown action. The availability of other units such as line drivers, J-K flip flops, R-S flip flops, and monostables will allow the designer to construct a complete logic system with a high degree of noise immunity throughout.

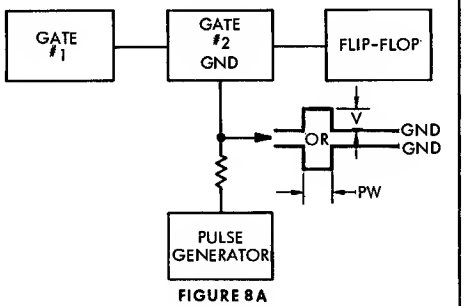


FIGURE 8A

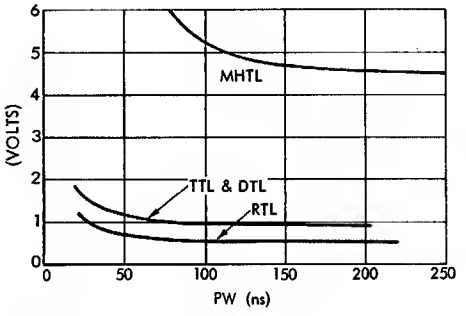


FIGURE 8B

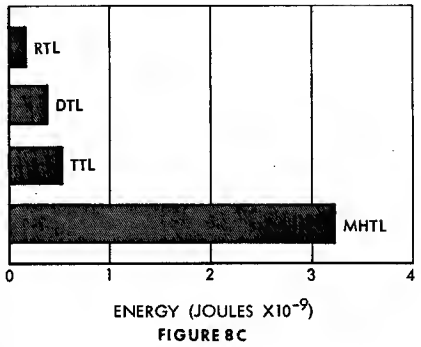


FIGURE 8C

GROUND LINE NOISE IMMUNITY

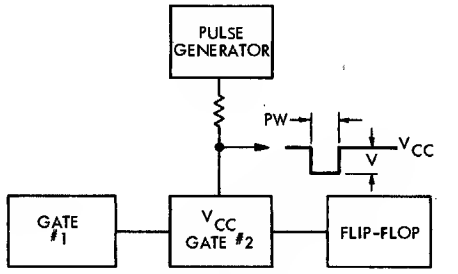


FIGURE 9A

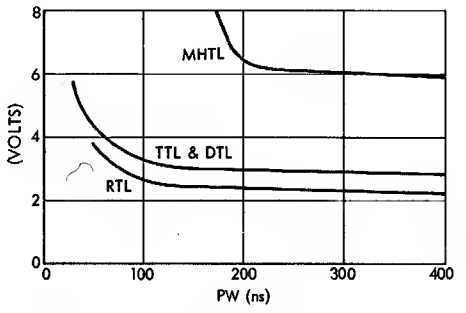


FIGURE 9B

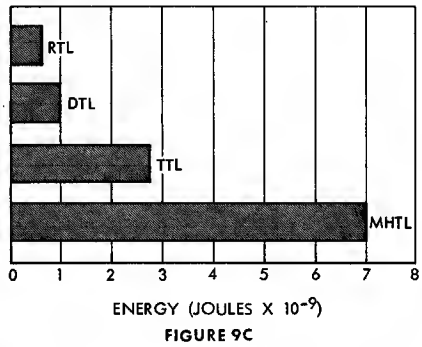


FIGURE 9C

POWER SUPPLY NOISE IMMUNITY

Situations arise where it would be advantageous to work into a system that operates at a higher speed than is obtainable by the high threshold devices. Translation between high threshold logic and standard logic families can be accomplished to allow the usage of high threshold devices as peripheral circuitry to a higher speed logic system. Thus, the high threshold devices may be operated in the noise environments and translation may take place into the lower threshold and higher speed system at the appropriate locations as indicated in Figure 10.

The higher supply voltage used in this logic family provides for the convenient interfacing with many discrete components. For example (Figure 11), the input may be controlled by a photo transistor so that illumination will cause the gate output to be high and darkness will provide a low output state. The output of the gate might feed into a logic system such that after a specific count would operate a relay. If a line driver unit were used as the output element, a 35mA, 15-volt relay could be employed. Other components such as lamps, SCRs, or transistors may also be driven directly at the output. As can be seen, the uses of the high threshold devices are many and varied.

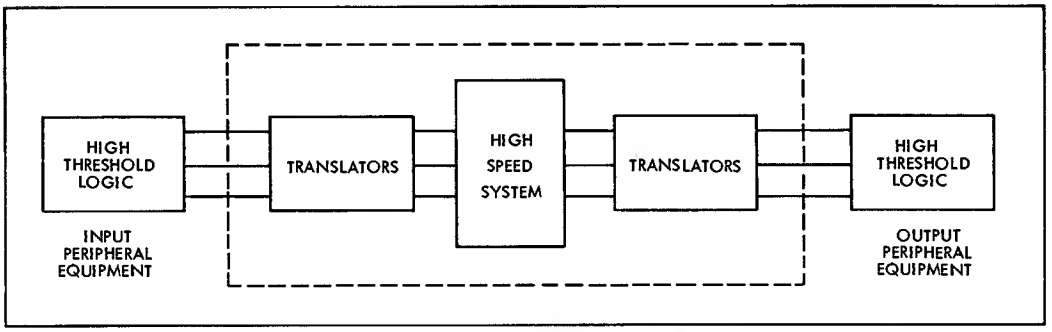


FIGURE 10 - OPERATING AS PERIPHERAL COMPONENTS

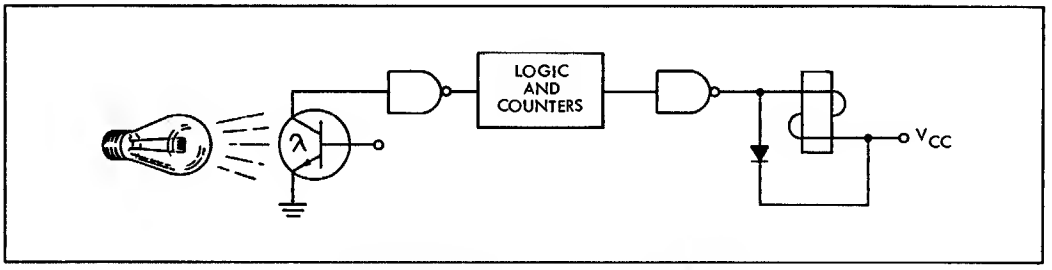


FIGURE 11 - OPERATING WITH DISCRETE COMPONENTS

SUMMARY

The new high threshold logic provides an integrated circuit logic family with a greater inherent immunity to electrical noise than is available with standard logic families. This logic family is ideal for situations where a large degree of electrical noise exists and where it is desirable to minimize the additional precautions necessary to reduce the effects of electrical noise. Input and output compatibility of the units with discrete components opens the door for a wide range of device employment.

OPERATION AND APPLICATION OF MHTL I/C FLIP-FLOPS

INTRODUCTION

The new High Threshold Logic (MHTL) line is designed to satisfy the requirements for systems that will operate in high electrical noise environments. The basic gate circuit of the family is essentially the same as the MDTL gate circuit with the coupling diode replaced by a reverse biased base-emitter junction which operates in the avalanche breakdown mode thus achieving a high input threshold. This family provides a positive logic NAND function or a negative logic NOR function.

Some typical characteristics of the family are:

- Single 15-volt power supply
- 7.5 V switching threshold
- 6-volt signal line noise margins
- 13-volt logic swing
- 30 mW gate power dissipation
- 100 ns gate propagation delay
- -30° to +75°C operating temperature range

Two flip-flops are currently available in the MHTL family, a dual J-K, the MC663P and a master-slave R-S, the MC664P. This application note describes the mode of operation of each flip-flop circuit in detail and will illustrate some typical uses of the devices.

MC663P DUAL J-K FLIP-FLOP

The MC663P unit contains two independent J-K flip-flops each with its own clock ($\overline{C}$) and direct reset ($\overline{R_D}$) terminals as shown in the block diagram of Figure 1A. Operation of the flip-flop in the synchronous or clocked mode follows the conditions shown in the Synchronous Truth Table in Figure 1B. The information on the J and K leads is effectively applied to the flip-flop when the clock lead is high and the output corresponds to the (n+1) truth table conditions upon the negative transition of the clock potential with commutation of the flip-flop occuring as the clock potential passes through the transition region (from 8.5 volts to 6.5 volts). The rise and fall times through these levels should not exceed 1 microsecond for proper operation. Clock pulse width at the 8.5 volt level should be greater than 200 nanoseconds, although typical units will operate with a 100 nanosecond pulse width. Operation in the synchronous mode requires that the direct reset inputs be terminated to V_{CC} if they are not used.

The direct reset terminal may be used to place the Q output in the 0 state independent of the steady state conditions on the J, K and $\overline{C}$ inputs. This is accomplished by

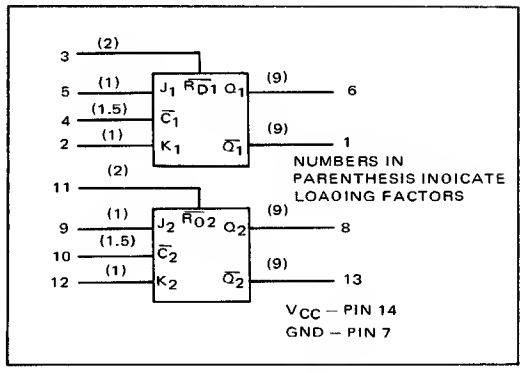


FIGURE 1A – MC663P BLOCK DIAGRAM

SYNCHRONOUS TRUTH TABLE

t_n		t_{n+1}	
J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	Q_n	$\overline{Q_n}$
1	0	1	0
0	1	0	1
1	1	$\overline{Q_n}$	Q_n

a. Direct input ($\overline{R_D}$) must be high.
b. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
c. 0 denotes low state, 1 denotes high state.
d. Q_n is the state of the Q output in the time period t_n.

DYNAMIC J-K TRUTH TABLE

J_n	K_n	J_{n+1}	K_{n+1}	Q_{n+1}
1	*	0	K_n	1
*	1	J_n	0	0
1	1	0	0	$\overline{Q_n}$
*	*	1	1	Q_n

* – Don't care.
n – Condition before change.
n+1 – Condition after change.
Clock and direct reset must be high.

FIGURE 1B – MC663P TRUTH TABLES

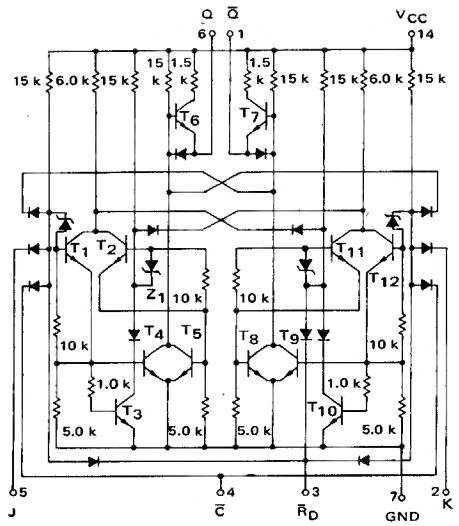


FIGURE 1C – CIRCUIT SCHEMATIC 1/2 MC663P

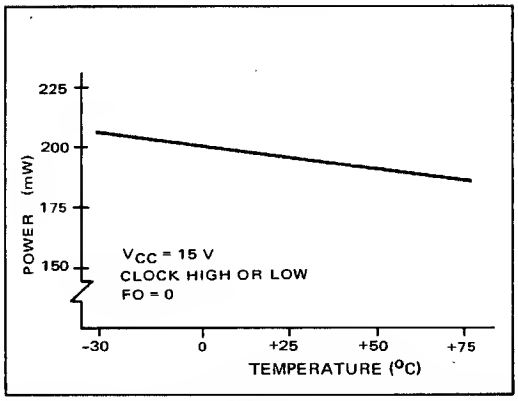


FIGURE 2A – TYPICAL MC663P POWER DISSIPATION versus TEMPERATURE

applying a logic zero to $\overline{R_D}$ for a period not less than 150 nanoseconds.

A third mode of operation may be achieved with these flip-flops as indicated in the Dynamic J-K Truth Table in Figure 1B. Operation in this mode requires the clock input as well as the direct reset input to be in the logic 1 state. Applying a logic 0 to the J and K inputs for a period greater than 150 nanoseconds will give the results indicated in the truth table. The rise time following an independent J or K negative excursion is not critical if the flip-flop remains in the given state; however, it should be less than 1 microsecond if both inputs are connected together when a logic 0 is applied or if the state of the flip-flop is changed by a negative transition on the other input. This characteristic will allow negative going signals to be capacitively coupled into the flip-flop when the J and K inputs are normally held high by external resistors.

Operation of the circuit will be explained using the schematic in Figure 1C. Initially, consider the following conditions: Q output in the low state and correspondingly the $\bar{Q}$ output in the high state, the clock input in the low state, and the direct reset input in the high state. Under these conditions, transistor T_6 will be off, transistor T_7 is on supplying current to any load connected to the $\bar{Q}$ output and T_5 is on, as will be explained later, sinking any load current on the Q output. Transistor T_2 is on with base current supplied through zener Z_1. Transistor T_2 being on supplies base current to T_5. All other transistors are off and this is the quiescent state for these conditions. If the clock input goes high and the J input is high or open, transistor T_1 turns on which also turns on T_3 and T_4. Transistor T_3 turning on will turn off T_2 which correspondingly turns off T_5. It should be noted that the output conditions have not changed due to the logical 1 on the clock input. The flip-flop will remain in this condition as long as the clock and J inputs remain high, but if either input goes low, the flip-flop will change state. If either the J or clock inputs go low, transistor T_1 turns off and its collector potential will rise causing T_{11} to turn on. T_{11} turning on supplies base current to T_8 and the $\bar{Q}$ out-

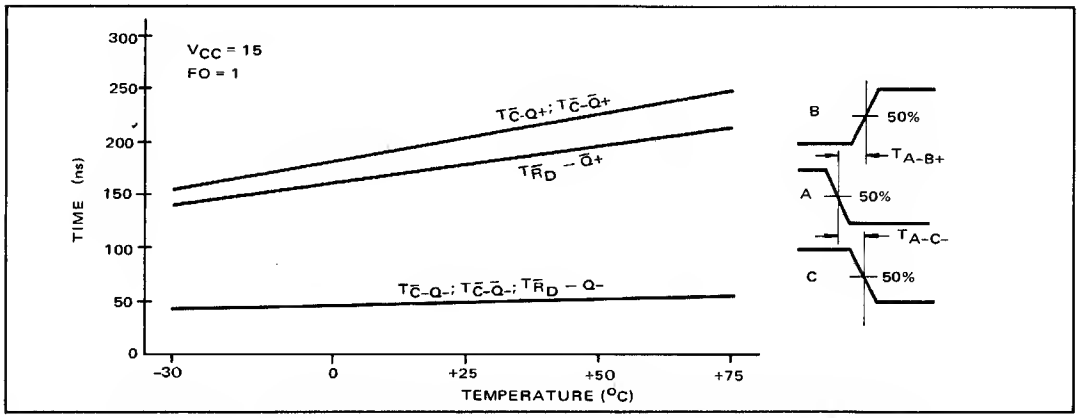


FIGURE 2B – TYPICAL MC663P PROPAGATION DELAY TIMES versus TEMPERATURE

put goes low. Transistors T_3 and T_4 are delayed in turning off after T_1 shuts off due to the charge stored in the base of T_4. Transistor T_3 being on prevents T_2 from turning on and T_2 will be held off once T_{11} turns on. Finally, when T_4 turns off, T_5 is also inhibited and the Q output goes high completing the flip-flop transition. A similar action will occur from this state to cause transition back to the original state if the clock and K input terminals are considered. It can be noted that commutation of the flip-flop may be inhibited by a logic 0 on the J and K inputs. This will prevent transistors T_1 or T_{12} from turning on when the clock is high and thus prevents commutation.

The flip-flop may be set to the Q = 0 state by use of the direct reset terminal $\overline{R_D}$ when the flip-flop is in the Q = 1 state. A logic 0 on $\overline{R_D}$ inhibits the J, K, and $\overline{C}$ inputs and will turn off T_{11} causing T_2 and T_5 to turn on placing the flip-flop in the Q = 0 state. T_{11} turning off removes the base current from T_8 and the $\overline{Q}$ output will go to the logic 1 level.

The load applied to the output terminals must be limited such that the output voltage will not be less than 8.5 volts when in the high state. This is necessary for proper cross-coupling between the two outputs of the flip-flop and the input circuitry.

Typical characteristics of the MC663P over the operating temperature range are provided in Figures 2A and B.

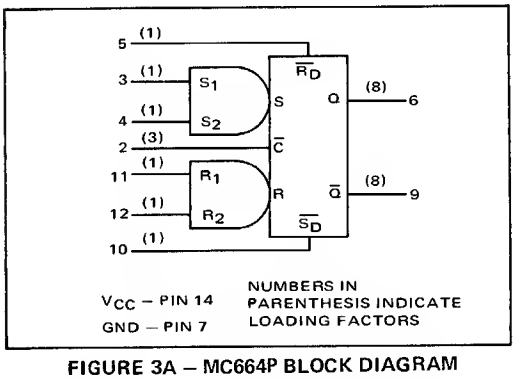


FIGURE 3A – MC664P BLOCK DIAGRAM

MC664P R-S FLIP-FLOP

The MC664P is a dc-coupled R-S flip-flop of the master-slave or two-phase type. Since it is an R-S type, simultaneous high inputs are not allowed because the output cannot be predicted after a negative clock transition. Information is entered in the master section while the clock pulse is high and is transferred to the slave when the clock goes negative.

The block diagram shown in Figure 3A indicates the logic function of the flip-flop as well as providing the loading factors for the device. The loading factor of 3 for the clock terminal is tested with the clock input at 1.5 volts. The output loading factors of 8 are reduced from the standard MHTL gate loading factor of 10 because of internal flip-flop cross connections.

CLOCKED OPERATION

t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

NOTES FOR CLOCKED-OPERATION TRUTH TABLE:
Direct inputs ($\overline{R_D}$, $\overline{S_D}$) must be high.
0 = low state
1 = high state
X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

DIRECT INPUT OPERATION

$\overline{R_D}$	$\overline{S_D}$	Q	$\overline{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

Clock ($\overline{C}$) input must be low
NC = No change
NA = Not allowed

FIGURE 3B – MC664P TRUTH TABLES

The truth tables for the circuit are provided in Figure 3B for both clocked operation and for the direct input terminals. It should be noted that the $\overline{R_D}$ and $\overline{S_D}$ terminals are high for clocked operation while direct set and reset requires the clock to be low.

The schematic for the MC664P is shown in Figure 3C. Operation of the circuit will be described by making the initial assumptions that the flip-flop is in the Q = 0, $\overline{Q}$ = 1 state, that the clock ($\overline{C}$) is low, and that the direct set and reset ($\overline{S_D}$, $\overline{R_D}$) terminals are high or open. Under these conditions, T_{10} and T_{13} would be off while T_8 and T_{11} would be on. Transistor T_9 is on and suppliesbase current to T_8 through the zener diode. For this situation to exist T_4 and T_5 would also be on, while the remaining transistors in the circuit are off. This indicates the quiescent condition for the flip-flop under the initial conditions.

To illustrate commutation of the flip-flop, assume that inputs S_1 and S_2 are open or high and that either R_1 and/or R_2 are low. Now, as the clock potential rises to approximately 7 volts, the first change to occur will be the conduction of T_7 which provides a second base current source to T_8 which is already on. A further increase in the clock potential of one forward V_{BE} magnitude will cause T_1 to turn on which turns on T_2. (It is noted that there is a V_{BE}

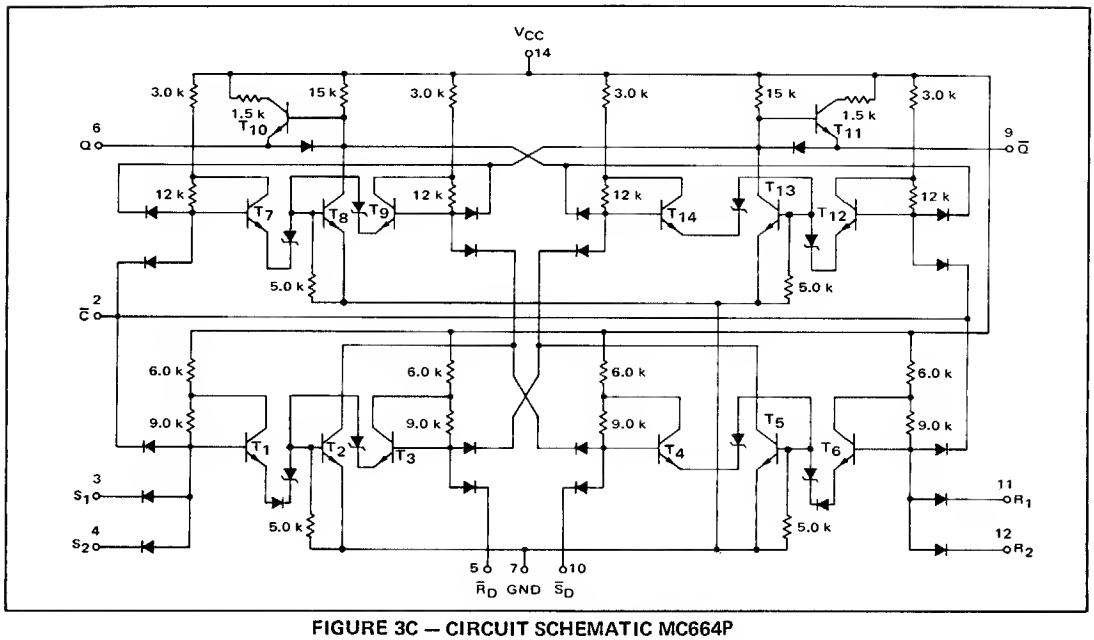


FIGURE 3C – CIRCUIT SCHEMATIC MC664P

diode offset between the master and slave sections of the flip-flop and it is essentially a dc rise time circuit.) Transistor T_2 turning on causes T_9, T_4 and T_5 to turn off. Transistor T_8 remains on, however, due to the second source of base current from T_7. Transistor T_5 being off causes T_3 to turn on and now T_2 is provided with base current from two sources. A continuing increase of the clock input will not cause any further changes in the flip-flop. As the clock potential starts to decrease, T_1 will turn off first although T_2 remains on due to the second base current source. When the clock potential falls an additional V_{BE} drop, T_7 and T_8 turn off and the Q output goes high. This high potential coupled with T_5 being off turns on T_{14} and T_{13} and the $\overline{Q}$ output goes low generating the changed flip-flop state. The conditions of the flip-flop will now remain the same for any further decrease in the clock potential. A similar action would return the flip-flop to the original state if R_1 and R_2 were high or open with S_1 and/or S_2 at the low level and a clocking waveform applied. Although information may be reliably applied to the flip-flop with essentially dc-risetime clock-waveforms, there is a point where the output rise and fall times are beta dependent on the clock level. This will increase the output transition times when excessively slow clock-waveforms are present.

The flip-flop state may be changed by use of the $\overline{R_D}$ and $\overline{S_D}$ terminals. If the condition is considered where Q = 0, $\overline{Q}$ = 1, $\overline{C}$ is low, and both $\overline{R_D}$ and $\overline{S_D}$ are high as in the preceding example, it can be observed that a momentary low on $\overline{S_D}$ will set the flip-flop to Q = 1, $\overline{Q}$ = 0. In this instance when $\overline{S_D}$ goes low, T_4 and T_5 turn off which causes T_3 and T_2 to turn on. With T_2 on, T_9 and T_8 turn off and the Q output goes high. This high potential coupled with T_5 being off, turns on T_{14} and T_{13} causing $\overline{Q}$ to go low completing the transition. Similar action results if the flip-flop were in the Q = 1, $\overline{Q}$ = 0 state and a momentary logical zero were placed on the $\overline{R_D}$ terminal.

A toggle mode of operation may be achieved with the flip-flop by connecting the Q output to one of the R inputs and the $\overline{Q}$ output to one of the S inputs. Under this condition, the truth table for synchronous operation of the MC663P would also apply to the MC664P by redefining the S input as the J and the R input as a K.

Power dissipation for this unit is typically 140 mW with V_{CC} = 15 V. Typical characteristics of parameters as a function of temperature are given in Figure 4A and 4B.

APPLICATIONS

Operation of the MC664P master-slave flip-flop is very similar to the MC931/831 flip-flop operation in the MDTL family. This fact, coupled with similar gate operation between the two families, allow construction of MHTL shift registers, counters and decoders in much the manner described in application notes covering the MDTL family (e.g., AN-235, 262, 283 and 284). The MC663P may be employed to take advantage of the dual function in many shift register and counter circuits, but with only the direct reset function available, parallel input operation is not as flexible as with the MC664P. Since the MC663P operates on a stored charge principle and different modes of operation may be obtained, the devices may be easily interconnected to form gateless ripple counters. Figure 5 illustrates several counters that may be constructed with a maximum

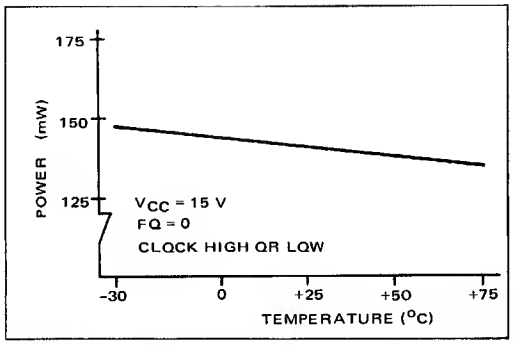


FIGURE 4A – TYPICAL MC664P POWER DISSIPATION versus TEMPERATURE

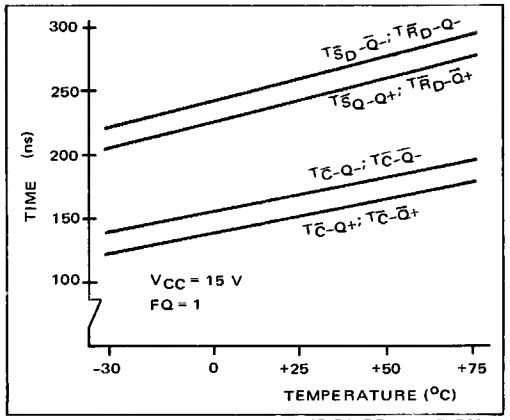
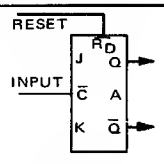


FIGURE 4B – TYPICAL MC664P PROPAGATION DELAY TIMES versus TEMPERATURE

of 2 MC663P Packages. It should be noted that direct resetting of these counters is independent of the clock level, consequently the reset time of any counter equals the reset time of a single flip-flop. The logic sequence and maximum signal ripple for each circuit is also provided in the figure.

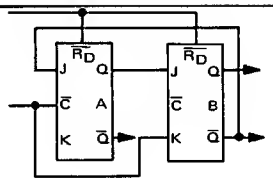
In Figure 6, a decade shift counter is constructed using 2 MC663P units and an MC664P for proper input gating. Typical waveshapes are illustrated for this connection and the necessary decoding logic is provided.



MAX RIPPLE–1

÷2

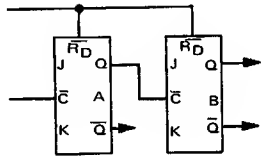
STATE	Q_A
1	0
2	1



MAX RIPPLE–2

÷3

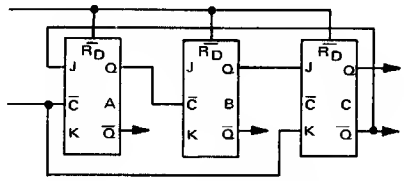
STATE	Q_A	Q_B
1	0	0
2	1	0
3	0	1



MAX RIPPLE–2

÷4

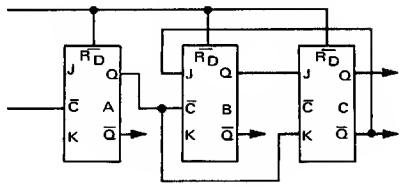
STATE	Q_A	Q_B
1	0	0
2	1	0
3	0	1
4	1	1



MAX RIPPLE–3

÷5

STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1

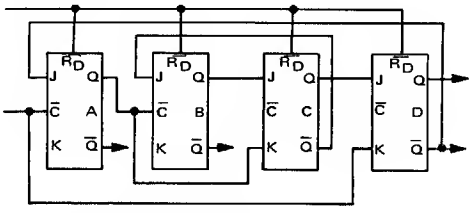


MAX RIPPLE–3

÷6

STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1

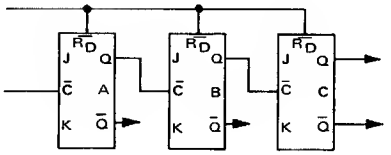
FIGURE 5 – GATELESS RIPPLE COUNTERS FROM MC663P DEVICES



MAX RIPPLE–3

÷7

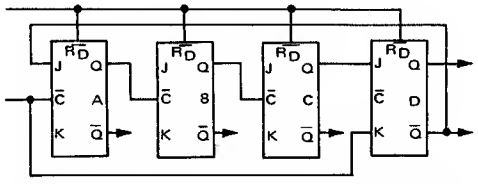
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	0	0	1



MAX RIPPLE–3

÷8

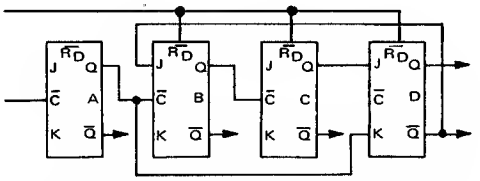
STATE	Q_A	Q_B	Q_C
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1



MAX RIPPLE–4

÷9

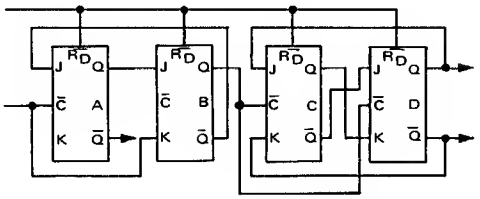
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1



MAX RIPPLE–4

÷10

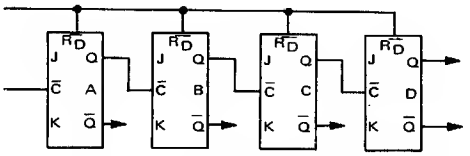
STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1



MAX RIPPLE–2

÷12

STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	0	0	0	1
5	1	0	0	1
6	0	1	0	1
7	0	0	1	1
8	1	0	1	1
9	0	1	1	1
10	0	0	1	0
11	1	0	1	0
12	0	1	1	0



MAX RIPPLE–4

÷16

STATE	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	1	0	0
5	0	0	1	0
6	1	0	1	0
7	0	1	1	0
8	1	1	1	0
9	0	0	0	1
10	1	0	0	1
11	0	1	0	1
12	1	1	0	1
13	0	0	1	1
14	1	0	1	1
15	0	1	1	1
16	1	1	1	1

FIGURE 5 – (continued)

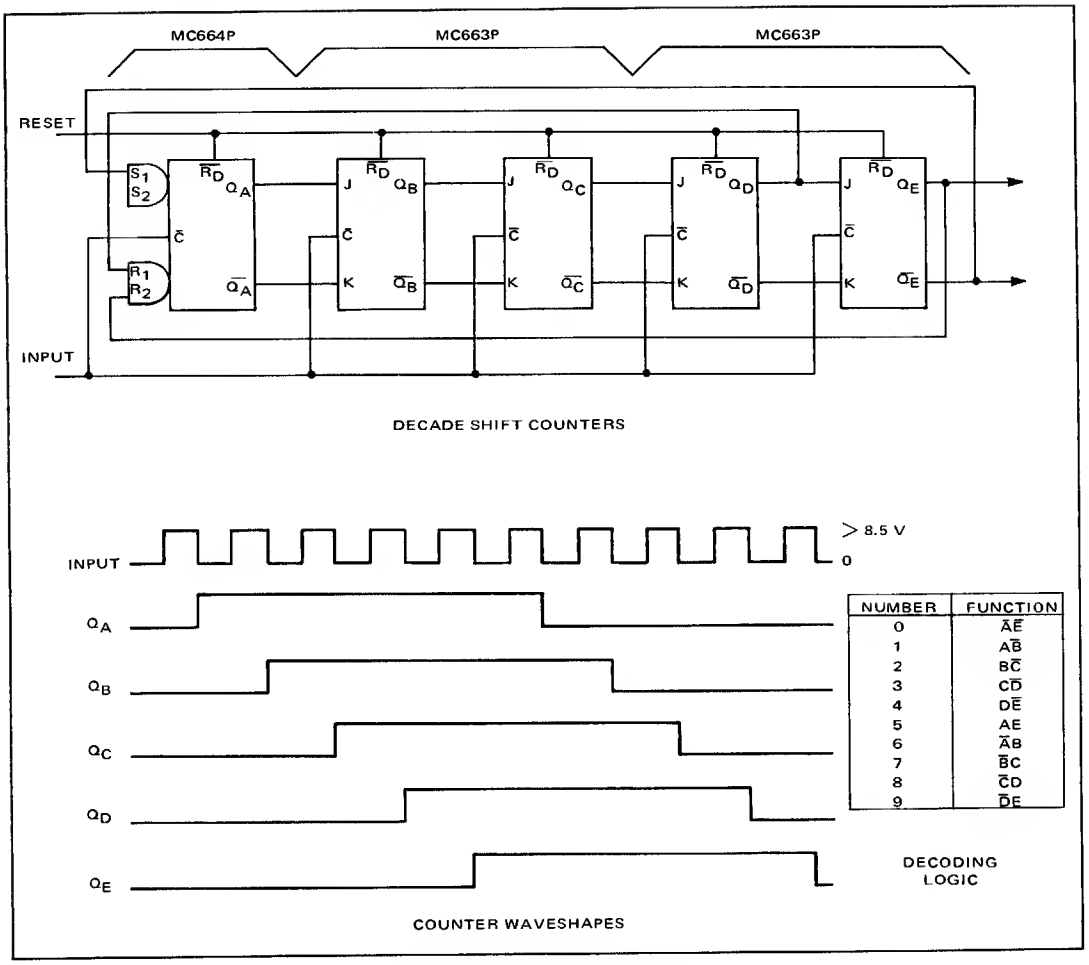


FIGURE 6 – DECADE SHIFT COUNTER AND COUNTER WAVESHAPES

CONCLUSIONS

The initial flip-flops in the MHTL family provide considerable flexibility for the design of digital electronic equipment to operate in environments subject to electrical noise. Some typical applications have been illustrated for usage of these MHTL flip-flops. In addition, a detailed explanation of operation of the devices has been given to help design the units into special applications.

AN INTEGRATED SENSE AMPLIFIER FOR CORE MEMORIES

INTRODUCTION

A definition of a sense amplifier could be "the interface circuitry between the storage elements of a memory and the logic output elements of the memory." By this definition, a sense amplifier can have many different type inputs and outputs. This paper will discuss a sense amplifier for ferrite core memories. Specific sense amplifier requirements were received from computer and core memory manufacturers. From these requirements, design goals were evolved for a sense amplifier that would satisfy the market.

An integrated sense amplifier offers advantages other than such obvious ones as saving weight, space, and assembly wiring; the inherent ability to match active components within the integrated circuit gives the integrated sense amplifier a distinct advantage over the discrete versions. In some cases, it would be very difficult to build a discrete circuit of the same quality as an integrated circuit, or to do so could be quite expensive. Therefore, a well-designed integrated sense amplifier will offer superior performance and be less expensive than its discrete counterpart.

THE CORE MEMORY

Figure 1 is a typical core memory subsystem of a general purpose digital computer. The appropriate x and y lines are selected by the memory address register (MAR). The selection technique depends on the memory organization and will not be discussed in this application note. The most common organizations use one core per bit so the number of cores which must be sensed simultaneously is determined by the "word" length. However, each sense line links one bit for all words in the memory. When a particular word is selected the sense amplifiers detect the presence of "ones" or "zeroes" in all the bits and this information is then placed in the memory data register (MDR). The time required to get the information from the cores to the MDR is called the "access" time. If the memory is of the "destructive readout" type, the information in the MDR must be written back into the memory at the same location. The time required to do this is called the "write" time. The sum of the "read" and "write" times is defined as the cycle time and indicates the speed of the memory.

The various memory organizations use different sense line configurations and current drive techniques. However, in all the configurations the sense winding is routed so as to obtain an optimum signal-to-noise ratio. This generally means the sense winding goes through half the cores in one direction and half in the opposite direction (See Figure 2). The purpose of this wiring technique is to

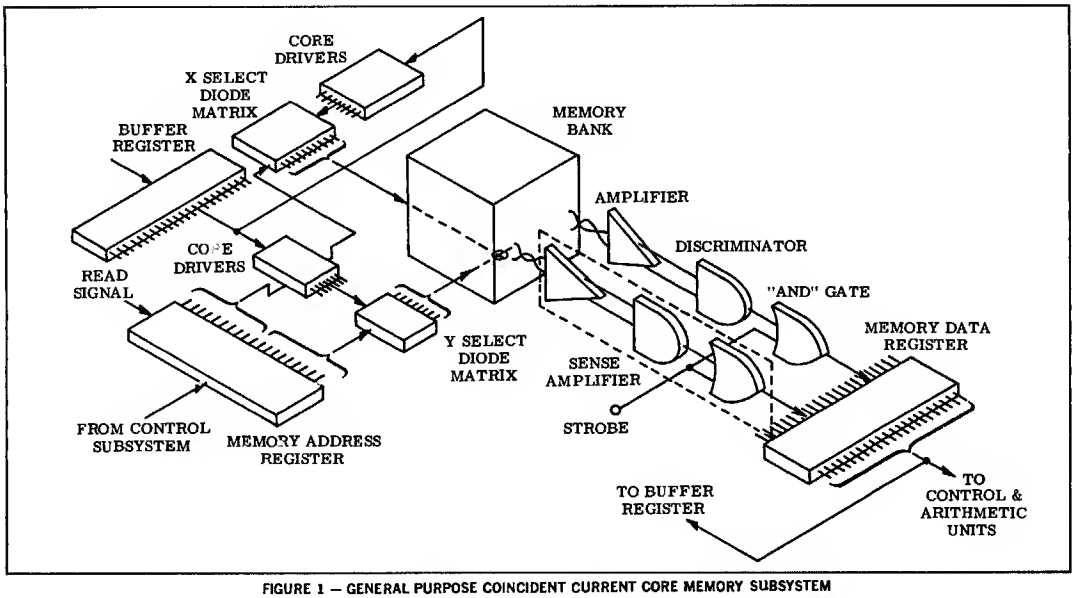


FIGURE 1 — GENERAL PURPOSE COINCIDENT CURRENT CORE MEMORY SUBSYSTEM

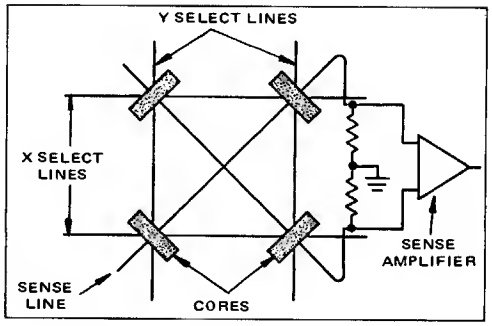


FIGURE 2 – HALF SELECT WIRING

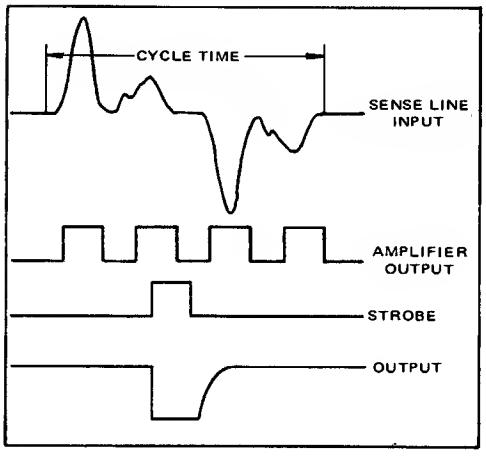


FIGURE 3a – TYPICAL SIGNAL WAVEFORMS

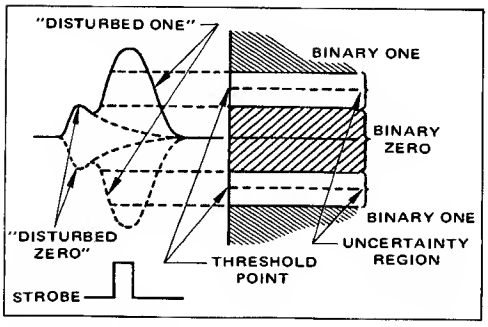


FIGURE 3b – TYPICAL CORE OUTPUT SIGNAL

cause voltages induced in the sense line to cancel. The sense amplifier must detect the difference between the minimum "disturbed one" signal and the maximum "disturbed zero" signal. The "disturbed one" signal can be either positive or negative so the sense amplifier must be bipolar (See Figure 3a).

Typical signal waveforms at the input to the sense amplifier, amplifier output, discriminator output, and strobe are shown in Figure 3a. This is an idealized signal waveform at the input to the sense amplifier. In actuality, there are common and differential mode noise at the input during most of the memory cycle. Figure 3b shows the typical signal as seen at the input to the sense amplifier. The amplitude of the "disturbed one" signal depends on the size of the core and the rise time and amplitude of the select currents from the core drivers. The area between the minimum "disturbed one" signal and the maximum sum of "disturbed zero" signals is called the uncertainty region (See Figure 3b). This area would ideally be as large as possible, since it is very important in the overall performance of the memory subsystem. Normally, the threshold of the sense amplifier will be set in the middle of the uncertainty region.

SENSE AMPLIFIER DESIGN CRITERIA

Many factors must be considered in the design of an integrated core memory sense amplifier. First, the amplifier should be as versatile as possible. The design must meet a wide variety of speed requirements and should be suitable for low cost fabrication. Additional criteria are:

1. The amplifier must be able to detect bipolar signals.
2. The threshold should be adjustable in order to meet the maximum number of requirements with a single amplifier.
3. The threshold should be constant with temperature. This requires the memory manufacturer to compensate the switching currents for the change in core output voltage rather than depend on the sense amplifier to have precisely the correct threshold versus temperature characteristic.
4. The uncertainty region should be as small as possible.
5. The power supplies should be commonly used values and the tolerances on these supplies should be as loose as possible.
6. The sense amplifier requires a strobe to "enable" the amplifier at the optimum point.
7. The bandwidth of the amplifier must be sufficiently high to pass the fastest rise time signals with as little degradation as possible.
8. The amplifier must be able to recover rapidly from large common mode and large differential mode signals.

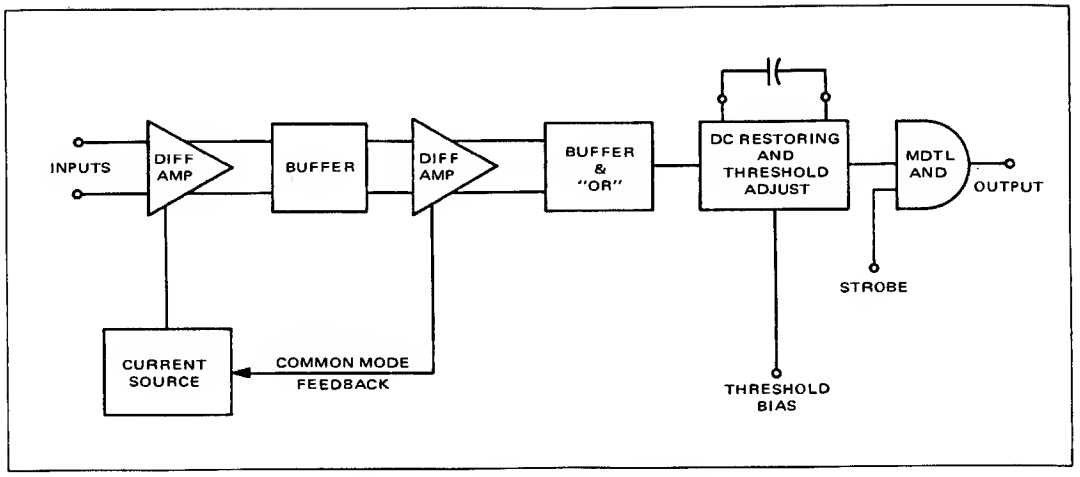


FIGURE 4 – BLOCK DIAGRAM OF MC1540

THE MC1540

Figure 4 is a block diagram of the MC1540. The amplifier portion is a two-stage differential amplifier with emitter degeneration in each stage, buffering between stages, and overall common mode feedback. The schematic of the amplifier section is shown in Figure 5. The low frequency differential voltage gain of the first stage, assuming it is driven from a voltage source, can be closely approximated by:

$$A_{diff} \approx \frac{R_L}{r_e + R_E + \frac{r_b}{\beta + 1}}$$

R_E is the emitter degeneration resistor on each side and r_e approximately $\frac{KT}{qI_E}$. With β relatively high, the last term in the denominator can be neglected and the equation for the gain reduces to the following equation:

$$A_{diff} \approx \frac{R_L}{r_e + R_E} = \frac{R_L}{R_E} \quad \frac{1}{1 + \frac{r}{R_E}}$$

This equation shows that the gain is a function of resistor ratios rather than resistor magnitudes. R_L and R_E are formed during the base diffusion so that the ratio R_L/R_E should be constant from run to run. Also, r_e is directly proportional to a resistor which is formed during the base diffusion and is a function of temperature so that gain variations with temperature change are to be expected. However, the gain variation will be significantly less than for a circuit with no emitter degeneration.

Since the amplifier incorporates differential gain of the first stage and single ended gain of the second stage, the overall gain can be approximated by the following equation:

$$A \approx \left(\frac{R_{L_1}}{r_{e_1} + R_{E_1}}\right) \left[\frac{R_{L_2}}{2(r_{e_2} + R_{E_2})}\right]$$

The buffering between the two stages significantly increases the bandwidth of the amplifier. Without buffering, the predominant pole would be caused by the Miller effect capacitance of the second stage being driven from a high impedance. Buffering reduces this impedance approximately by a factor of β of the transistor.

Some of the data taken on this amplifier in integrated form is shown below.

1. Voltage gain – The voltage gain on all units was between 37.5 dB and 40 dB.

2. Gain versus temperature – The gain changed less than 1.0 dB when the temperature was varied over a -55°C to +125°C range.

3. Bandwidth – The 3.0 dB point on all units was in excess of 50 MHz. The rise time of the amplifier was less than 7.0 ns.

4. Propagation delay – This was found to be between 8.0 and 11.0 ns on all units. The measurement was made between the 50% points of the input and the output waveforms. The rise and fall times of the input were approximately 10 ns and the amplitude was 25 mV.

5. Common mode rejection – The low level common mode rejection defined as the differential mode gain divided by the common mode gain, was found to be 57.0 dB at 10 MHz. Figures 6a and 6b show the amplifier response to a ± 1.0 volt and a ± 2.0 volt common mode input respectively. Figure 6c shows the amplifier response to a 20 mV differential input.

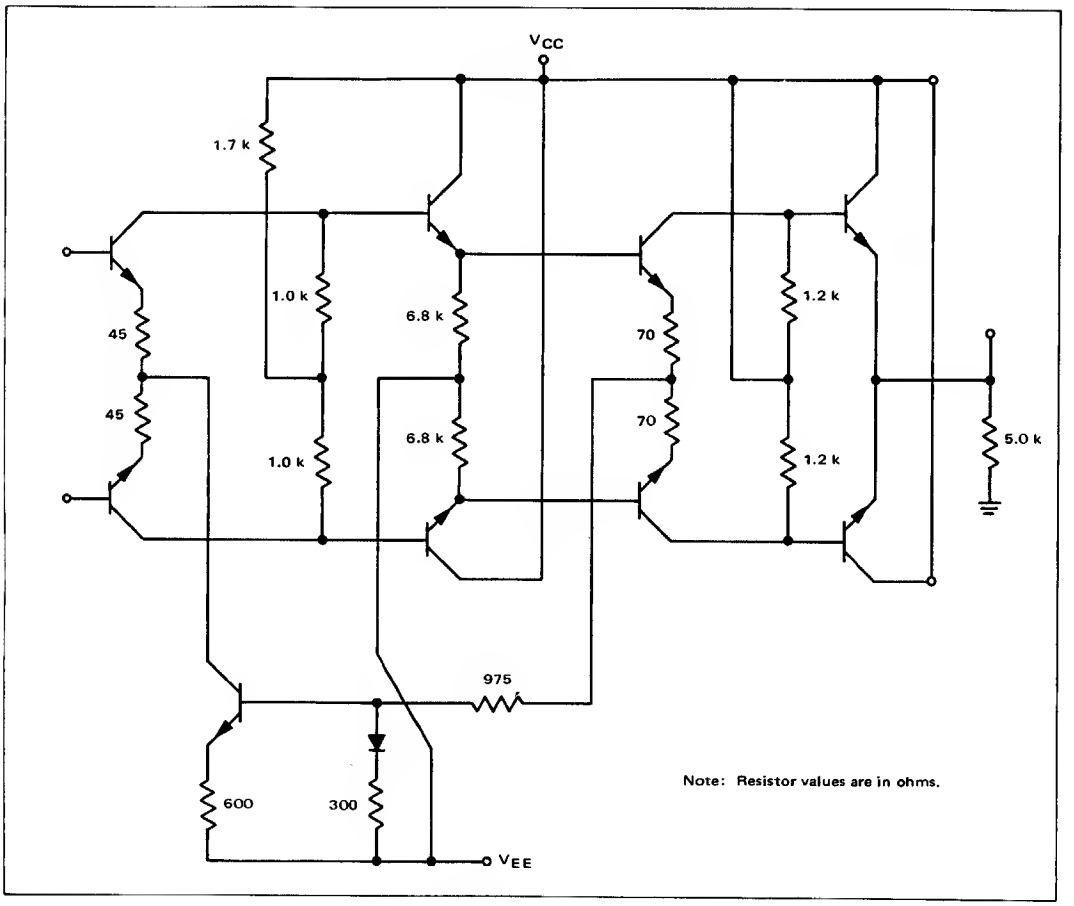


FIGURE 5 – DIFFERENTIAL AMPLIFIER SCHEMATIC

The schematic of the dc restoration circuit, the threshold adjusting circuit, and the output gate is shown in Figure 7. The threshold of the sense amplifier is dependent upon the dc voltage at point A. Since R1 is much larger than R2 or R3, changes in the dc voltage at point C reflects as a dc voltage change at point A; thus, the threshold changes.

The dc restoration action can be explained as follows: The input signal to the collector of Q_1 and the capacitor is positive from a low impedance and the entire signal is coupled through the capacitor. When the leading edge of the signal occurs at point A, both the base-emitter junctions of Q_1 and the gate input diode become reverse biased and the capacitor will start to charge through R4. When the negative going edge of the signal arrives at point A, Q_1 is turned on, and point A becomes a low impedance node because of the emitter follower action. The capacitor will discharge through Q_1 very rapidly. The base of Q_1 is driven by a low impedance source so that the transient base current during the time the capacitor is being discharged produces a negligible voltage change at the base of Q_1. Also Q_1 is designed to supply the maximum transient current required for pulse widths up to 750 ns. Since the dc level at the emitter of Q_1 is restored rapidly, the sense amplifier threshold does not change significantly with a change in duty cycle.

As temperature increases, the threshold of the DTL gate decreases by $2\ \Delta V_{BE}/^{o}C$. The four diodes in the base of Q_2 will decrease the dc level at the base of Q_2 by $4\ \Delta V_{BE}/^{o}C$. The V_{BE} change of Q_1 will cancel one of these, and the V_{BE} change of Q_2 will cancel another; hence the dc level at point A will also decrease by $2\ \Delta V_{BE}/^{o}C$. Therefore, if the amplifier voltage gain does not change with temperature, the sense amplifier threshold will be constant.

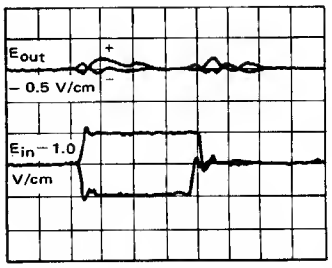


FIGURE 6a –
COMMON MODE RECOVERY
TIME (E_{in} = ± 1.0 V)

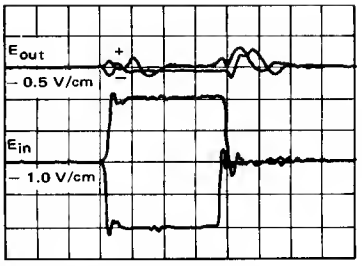


FIGURE 6b –
COMMON MODE RECOVERY
TIME (E_{in} = ± 2.0 V)

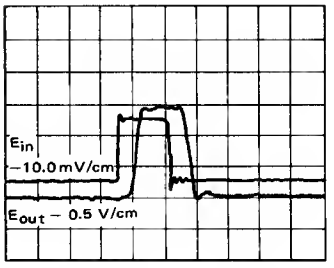


FIGURE 6c –
AMPLIFIER RESPONSE TIME

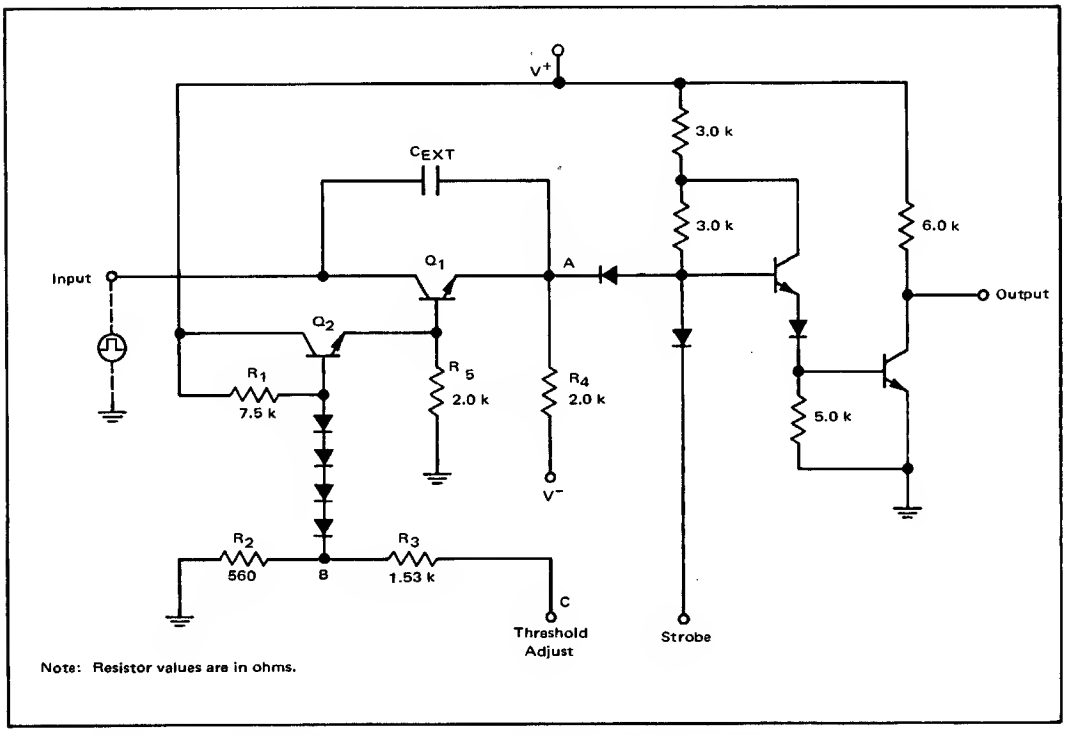


FIGURE 7 – DC RESTORATION CIRCUIT, THRESHOLD ADJUSTING CIRCUIT, AND OUTPUT GATE

The output gate is similar to that of the popular MDTL logic family. Both the amplified signal from the memory and the strobe signal must be above the gate threshold level before the output transistor will saturate. The output transistor is capable of "sinking" 6.0 mA with a saturation voltage less than 400 mV. This guarantees a noise margin equal to that of the MDTL logic family. Many sense amplifiers may be strobed from a common source with no ill effects, as long as the driving unit has sufficient fan-out capability. Also the outputs of several sense amplifiers can be wire-ORed. Figure 8 shows the voltage transfer characteristic of the gate. The width of the transition is approximately 200 mV. This would refer to the input of the sense amplifier as a transition width of 2.0 mV if the voltage gain was 100.

Additional data taken on the sense amplifier are listed below.

1. Threshold – 17 mV nominal for $V^- = -6.0$ V, $V^+ = +6.0$ V, and $V_{th} = -6.0$ V.
2. Threshold temperature coefficient – $-10\ \mu V/^oC$.
3. Threshold range – The nominal threshold varies from 13 mV at -5.0 V threshold bias to 21 mV at -7.0 V threshold bias.
4. Propagation delay from input to output – Typically 20 ns.
5. Propagation delay from strobe input to output – Typically 10 ns.

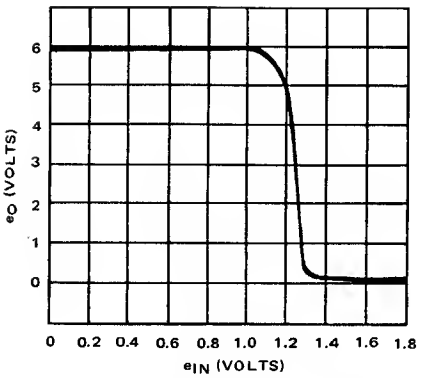


FIGURE 8 – OUTPUT GATE TRANSFER CHARACTERISTICS

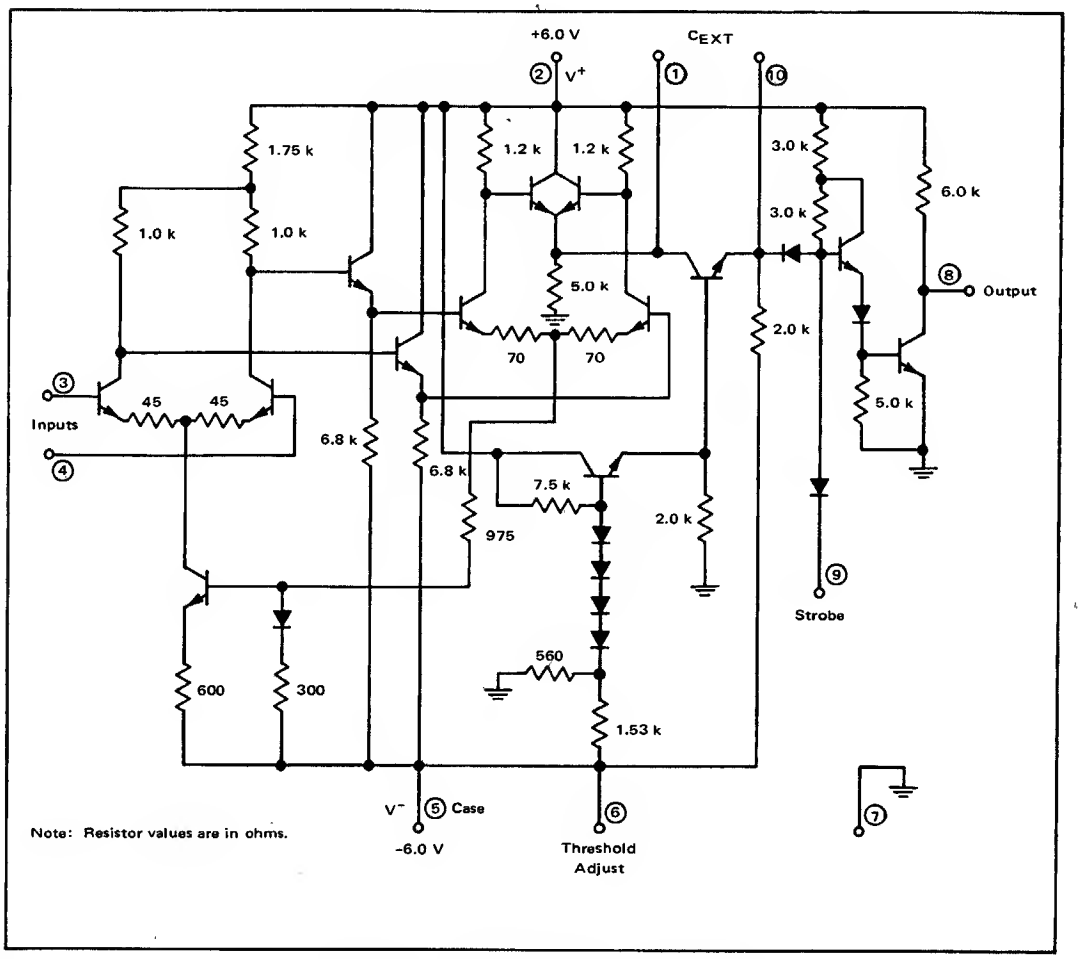


FIGURE 9 – CORE MEMORY SENSE AMPLIFIER

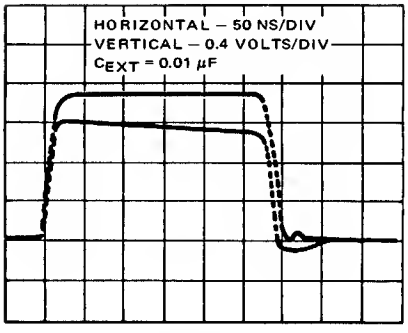


FIGURE 10 – SIGNAL WAVEFORM AT PINS ONE AND TEN

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Threshold	V_{th}	14	17	20	mV
Uncertainty Region			2	6	mV
Amplifier Voltage Gain	Av		80		
Propagation					
Input to Amplifier Output	$t_{3^+10^+}$			15	ns
Input to Gate Output	$t_{3^+8^-}$			30	ns
Strobe to Gate Output	$t_{9^+8^-}$			15	ns
Recovery Time					
e_{in} = ±400 mV (DM)	tr (DM)		20	50	ns
e_{in} = ±2.0 volts (CM)	tr (CM)		40	50	ns

Figure 9 is the schematic of the complete sense amplifier. External components that must be supplied are appropriate resistors for terminating the sense windings and a coupling capacitor. The size of the capacitor is dependent on the width of the disturbed "1" signal from the memory. The capacitor should be of sufficient size to ensure that the "sagging" due to the capacitor charging does not affect the threshold. Also the capacitor must be large enough so that noise, just before the disturbed "1" signal, does not affect the threshold. Figure 10 illustrates the charging and discharging time of a 0.01 μF capacitor. The typical excursion below the base line is approximately 100 mV for an input pulse 300 ns wide.

The rise time of the output can be decreased significantly by connecting an external resistor from the output to the positive power supply. This resistor must be large enough so that the sum of the current through the resistor and the current from an external load does not exceed the rated value of 6.0 mA if a 400 mV V_{sat} at +125°C is a required specification.

The sense amplifier also works fine with +5.0 V and -6.0 V power supplies. If the threshold-adjust pin is also tied to -6.0 V, the nominal threshold increases to approximately 20 mV. However, -5.3 volts on the threshold-adjust pin sets the nominal threshold at 17 mV for +5.0 V and -6.0 V power supply operation. If the threshold-adjust pin is tied to the negative power supply, the nominal threshold is also 17 mV for power supplies of +5.0 V and -5.0 V. Operation is marginal for ±4.5 V power supplies. Therefore it is recommended that ±5% supplies be used if the sense amplifier is operated with ±5.0 V power supplies.

SPECIFICATIONS

Specifications for a sophisticated integrated circuit must be such that the customer is guaranteed a circuit that will meet his requirements. The most important specifications for a sense amplifier are threshold limits (or uncertainty region), propagation delays, and recovery times. Other characteristics must also be limited so that good circuit performance and reliability result.

Some of the important specifications for the MC1540 are listed in the table above. For a complete specification and the manner in which each test is made, refer to the MC1540 data sheet.

SUMMARY

The MC1540 was designed with both customer requirements and integrated circuit production capabilities in mind. The circuit will operate properly with large variations in temperature and power supplies. It requires only three external components to achieve the complete core memory sense amplifier function. It has a saturated logic type output and can be strobed from any saturated logic family. It can be packaged in either the 10 pin TO-5, the 10 pin ceramic flat pack, or the dual in-line plastic package.

TRANSISTOR LOGARITHMIC CONVERSION USING AN INTEGRATED OPERATIONAL AMPLIFIER

INTRODUCTION

Many approaches have been made to the design of logarithmic amplifier circuits, using both active and passive elements. With the proper circuit configuration of diodes or transistors a log amplifier can be constructed using the logarithmic characteristics of these semiconductor devices. All diodes and transistors do not exhibit good logarithmic characteristics, so care must be taken in selecting the proper device. This application note deals with a technique for obtaining logarithmic conversion using operational amplifier-transistor feedback circuits, beginning with an analysis of the logarithmic characteristics of transistors. A brief look at the basic logarithmic amplifier will be given followed by two log function generator applications: direct multiplication of two numbers, and solution of the parabolic equation $Z = X^n$.

TRANSISTOR LOGARITHMIC CHARACTERISTICS

Shockley's first-order theory of a p-n junction

$$I = I_o [e^{(qV/kT)} - 1]$$

considers only diffusion current; however, it is popular because of its simplicity. In other circumstances the series resistance associated with the bulk semiconductor material must be accounted for. Also such mechanisms as surface inversion layers and generation-recombination in the space charge regions are not accounted for in the above expression. Consequently a diode or transistor configuration must be devised which will minimize these adverse effects. The common base transistor configuration discussed in this application note does this very well. By using the transfer conductance and fulfilling certain conditions, the desired logarithmic characteristics can be obtained.

The derivation of the transfer conductance is based around an NPN silicon all-diffused transistor as shown in Figure 1. The detailed derivation is given in the Appendix. The resulting collector current expression is

$$I_c = -\alpha_n I_{es} [e^{qV_E/kT}] \qquad (1)$$

It is important to note that a non-constant base transport factor will cause α_N to vary, consequently, a diffused base transistor such as the 2N2218 is best suited for this application. The base transport factor is within a few tenths of a percent of unity. The upper end range of equation (1) is usually between 1 and 10 mA of collector current depending upon the junction area and contact size of the transistor being used. Measurements elsewhere[1] indicate an 8 to 10 decade range of collector current yielding a logarithmic relation. Simple practical integrated circuit operational amplifiers operating with only a single polarity input are limited to from 3 to 7 decades depending upon the particular amplifier being used and also on the effort expended to reduce external disturbances.

LOGARITHMIC AMPLIFIER TRANSFER FUNCTION

The basic function generator configuration for logarithmically compressing data is shown in Figure 2. In this configuration the requirement that the collector voltage be equal to zero is virtually met. The small amount of collector potential that does exist will be negligible for all practical purposes. Rewriting equation (1) for the direction of collector current shown in Figure 2, we find

$$I_c = +\alpha_n I_{es} [e^{qV_E/kT}] \qquad (2)$$

If $I_b \ll I_c$, which is the condition that governs the lower limit of operation, then

$$I_c = \frac{E_{in}}{R_s} \qquad (3)$$

The polarity of V_E is shown in Figure 2. Combining equations (2) and (3) and the condition of $V_{out} = V_E$ yields

$$\frac{E_{in}}{R_s} = \alpha_n I_{es} [e^{qV_{out}/kT}]$$

or

$$V_{out} = \frac{kT}{q} \ln \frac{E_{in}}{R_s \alpha_n I_{es}}$$

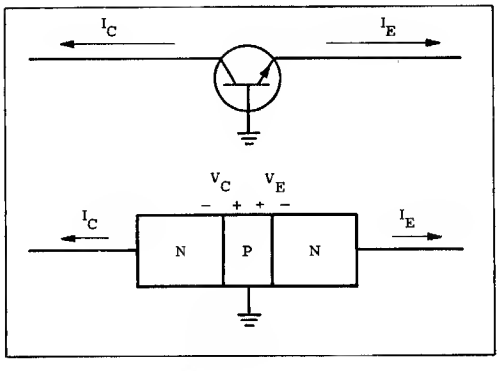


FIGURE 1 — NPN SILICON TRANSISTOR MODEL

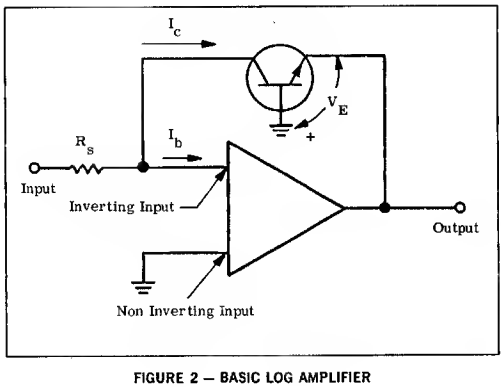


FIGURE 2 — BASIC LOG AMPLIFIER

Converting from $\ln_e$ to $\log_{10}$ gives

$$V_{out} = 2.3 \frac{kT}{q} \log_{10} \left(\frac{E_{in}}{R_s \alpha_n I_{es}}\right)$$

$$V_{out} = 2.3 \frac{kT}{q} \log_{10} (E_{in}) + 2.3 \left(\frac{kT}{q}\right) \log_{10} \left(\frac{1}{R_s \alpha_n I_{es}}\right) \quad (4)$$

at $T = 27°C$ $\quad \frac{kT}{q} = 0.026\,V$

$$V_{out} = 0.06 \log_{10} (E_{in}) + K \quad (5)$$

The empirical results obtained from the log amplifier are plotted in Figure 3a. From Figure 3a the transfer function was found to be

$$E_{out} = 0.062 \log_{10} (E_{in}) + 0.450 \quad (6)$$

where E_{out} and E_{in} are in volts.

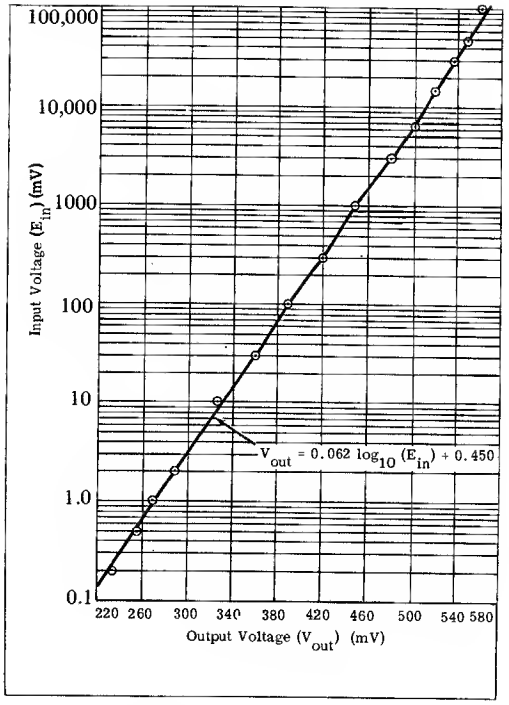


FIGURE 3a — INPUT VS. OUTPUT RESPONSE OF LOGARITHMIC AMPLIFIER OF FIGURE 3b

OPERATIONAL AMPLIFIER LOG AMPLIFIER

The operational amplifier used in the log amplifier is the MC 1533. Frequency compensation of the operational amplifier is chosen such that the amplifier will be stable with a closed loop gain of unity. The 0.1 μF capacitor between pins 1 and 5 is necessary to reduce the ac gain of the feedback transistor. It is usually necessary to bypass the power supplies right at the amplifier socket with a 0.01 or 0.1 μF low-inductive capacitor to eliminate any internal high frequency oscillations which might occur because of excessive impedance in the power supplies.

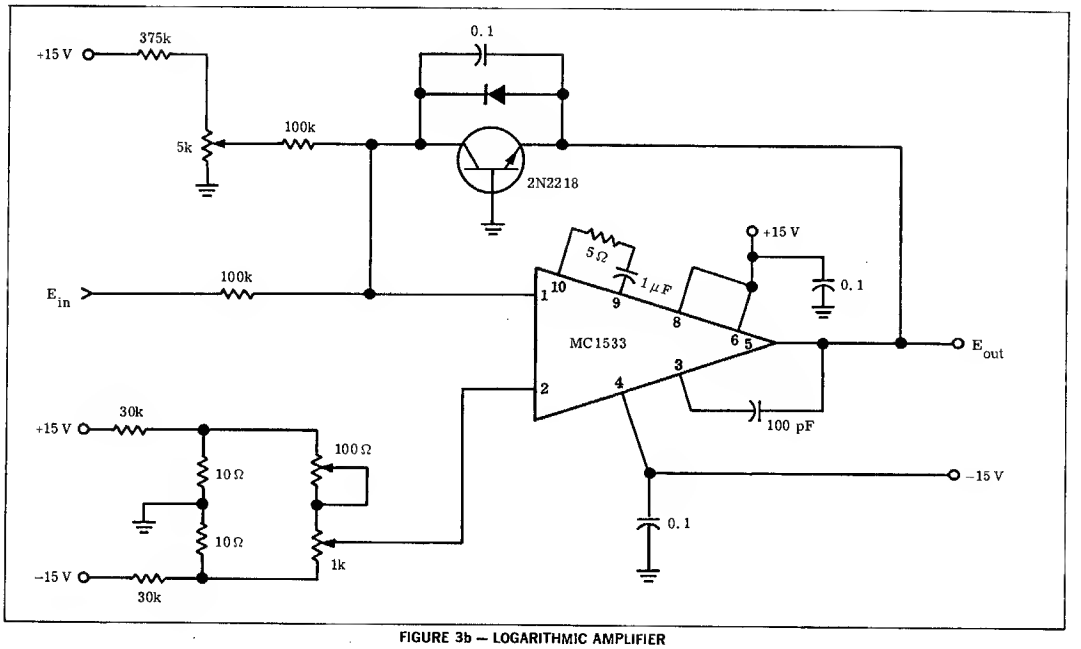


FIGURE 3b — LOGARITHMIC AMPLIFIER

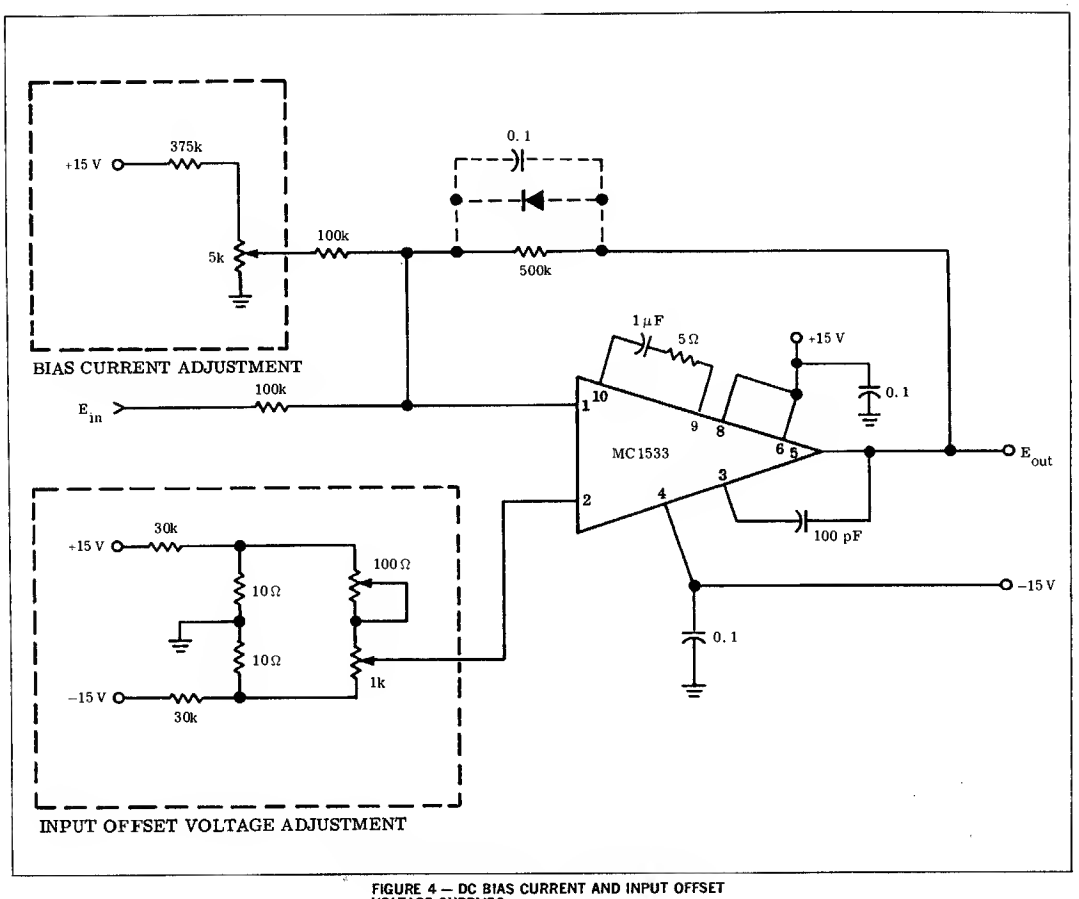


FIGURE 4 — DC BIAS CURRENT AND INPUT OFFSET VOLTAGE SUPPLIES

The extremely wide range of input voltage required makes it necessary that input offset voltage and bias currents be properly compensated for. The typical bias current for the MC 1533 is 0.5 μA. If the amplifier were used without proper bias current compensation, this would require an input voltage of 50 mV above a 100k input resistor just to overcome the bias current requirements. This would immediately swamp out the lower end input of a 4 to 5 decade log amplifier where input voltages are in the 1 to 10 mV range. Input offset voltage, which is reflected to the output by the closed loop gain of the amplifier, will cause an appreciable error, and must be compensated for with an external supply.

The method of dc compensation used is shown in Figure 4. The input offset voltage adjustment is made with pin 1 shorted to ground and E_{out} adjusted to zero. The bias current adjustment is accomplished by placing a 500k feedback resistor in place of the transistor and then monitoring E_{out} and E_{in} and adjusting the bias current pot until E_{out}/E_{in} = 500k/100k = 5 throughout the desired input range. This procedure must be carried out individually for each operational amplifier that is to be used as a log amplifier. After completion of the bias adjustments, the feedback resistor may be replaced by the feedback transistor in the configuration shown in Figure 3b.

The same type of bias current compensation is required in the $\log^{-1}$ amplifier where input voltage levels are in the 300 to 600 mV range. The offset voltage adjustment, however, may be replaced by approximately 100 ohms to ground, since the offset level is insignificant with respect to the input voltage range.

The effect of having an improperly adjusted offset voltage pot or bias current pot is demonstrated in Figure 5. It may be necessary to slightly adjust the bias current pot in order to straighten out the log characteristics, even after the initial adjustment procedure. It is extremely important in applications where log-analog operations are to be performed, that the logarithmic transistors have identical characteristic slopes. Level shifts are not important, since they can be easily adjusted for at the summing point of one of the internal amplifier stages as shown later in the multiplier circuit application.

MULTIPLICATION USING TRANSISTOR LOGARITHMIC CHARACTERISTICS

The following example explains a method of obtaining the product Z = XY. The circuit used is shown in Figure 6. The inputs and output are monitored in millivolts and the scale is selected such that one machine unit equals 10 mV. The circuit can be broken into three por-

tions: the input logarithmic amplifier, the summing point amplifier, and the output $\log^{-1}$ amplifier. The frequency compensation for each amplifier is the same as that shown in Figure 3b.

A. Input Logarithmic Amplifier: Each input in this portion of the product function generator is identical to that shown in Figure 4, with the feedback resistor replaced by the log transistor. Initial adjustments must be carried out in the same manner as discussed previously. The output of amplifier #1 will be of the form

$$E_{out(1)} = -(\text{alog } X + C_1) \tag{7}$$

and amplifier #2 will be identical except for the constant C_1

$$E_{out(2)} = -(\text{alog } Y + C_2) \tag{8}$$

The constants C_1 and C_2 are in the order of 300 mV while a = 62 as determined previously from Figure 3a.

B. Summing Point Amplifier: The output of this amplifier will be

$$E_{out(SPA)} = \text{alog } X + \text{alog } Y + C_1 + C_2 - E_c$$

$$= \text{alog } XY + C_1 + C_2 - E_c \tag{9}$$

The input required for the output $\log^{-1}$ amplifier stage must be of the form alog XY + C_3. With the proper selection of E_c the term $C_1 + C_2 - E_c$ can be made equal to C_3, resulting in the required input of the $\log^{-1}$ amplifier stage.

C. Output Log^{-1} Amplifier: This stage uses a 2N2906 transistor connected in a common base configuration at the input of the operational amplifier to achieve an anti-logarithmic amplifier. This stage must have a base current supply added to avoid having base current drawn from the input voltage. Distortion in the $\log^{-1}$ characteristic would result without this supply. The initial calibration of this stage must be determined by plotting input voltage $E_{in(OLA)}$ versus output voltage on semi-log paper and adjusting the 5 k base current pot until a straight line is obtained over the desired output range.

The results obtained from this circuit configuration are tabulated in Table 1 along with the correct product and percent error. Up to 7.7% error in output voltage was observed over the 3 decades of operation; however, simple calculations indicate that a 0.35% error in $E_{in(OLA)}$ will cause a 10% error in output voltage at the upper end of the output range. A 0.51% error in $I_{in(OLA)}$ will cause a 10% error in output voltage at the lower end of the output range. It becomes apparent why both an input offset voltage adjustment supply and a base current adjustment supply must be provided for where wide ranges of input or output voltages are to occur.

ANALOG SOLUTION OF THE PARABOLIC $= X^n$ EQUATION $Z = X^n$

The circuit shown in Figure 7 was used to generate Z for three different values of "n" (3, 2, and 0.5). The results are shown in Figures 8, 9, and 10, respectively. The value of E_c (summing point amplifier) is positive for n > 1 and negative for n < 1. As shown in Figure 7, E_c is positive and "n" is equal to 3. It is important here that the ratio of R_f/R_S be selected accurately to avoid additional error in the computation of X^n. The degree of accuracy maintained was 8% for "n" = 3, 9% for "n" = 2, and 5% for "n" = 0.5. As in the output stage of the previous application, a very small percentage error in input will increase more than an order of magnitude at the output.

Temperature variation will cause large deviations in output voltage accuracy since the output voltage of the first stage is directly proportional to temperature in degrees Kelvin.

$$E_{out(1)} = T[2.3(\frac{k}{q})\log_{10}(E_{in}) + 2.3(\frac{k}{q})\log_{10}(\frac{1}{R_S \alpha_n I_{Es}})]$$

The temperature effect will cancel itself if the junction temperatures of the input and output transistors are kept equal. Methods of obtaining the required temperature equalization might be the use of a common heatsink for all the log transistors, use of multiply packaged transistors, or ultimately the use of a monolithic chip containing the logarithmic transistors. A multiply packaged transistor MD 985 (PNP-NPN) was tried in the $Z = X^3$ configuration and resulted in an output error reduction of from 8% maximum to 4% maximum.

CONCLUSION

A diffused base transistor operating in a common base emitter follower configuration, with the collector at zero potential, has a wide range of logarithmic impedance. This configuration can be used to obtain a logarithmic compression of input data over 6 decades of operation with an error of less than 1%. The author feels that additional range could be obtained by the use of a chopper stabilized operational amplifier. Two arithmetic problem solution applications were shown; however, accuracy was limited by temperature variations, interstage inaccuracies, and resistor ratio inaccuracies over the three decades of input and output swing. A monolithic configuration of log transistors is felt to be the best method of compensation for temperature effects.

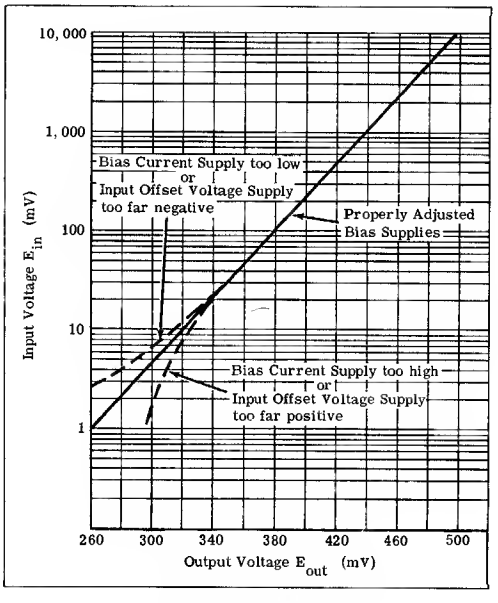


FIGURE S — IMPROPER DC COMPENSATION EFFECTS

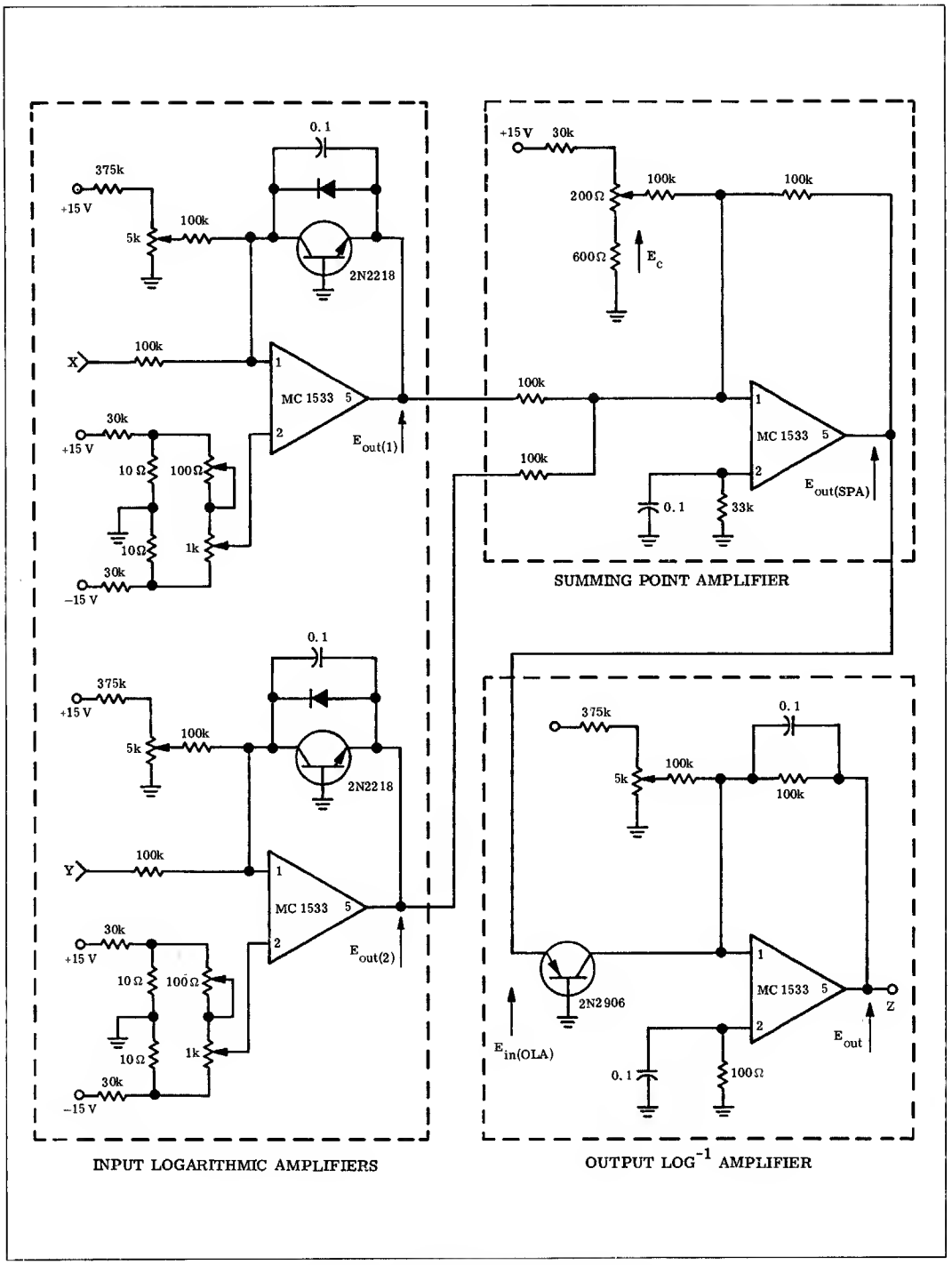


FIGURE 6 — CIRCUIT FOR Z = XY FUNCTION GENERATOR

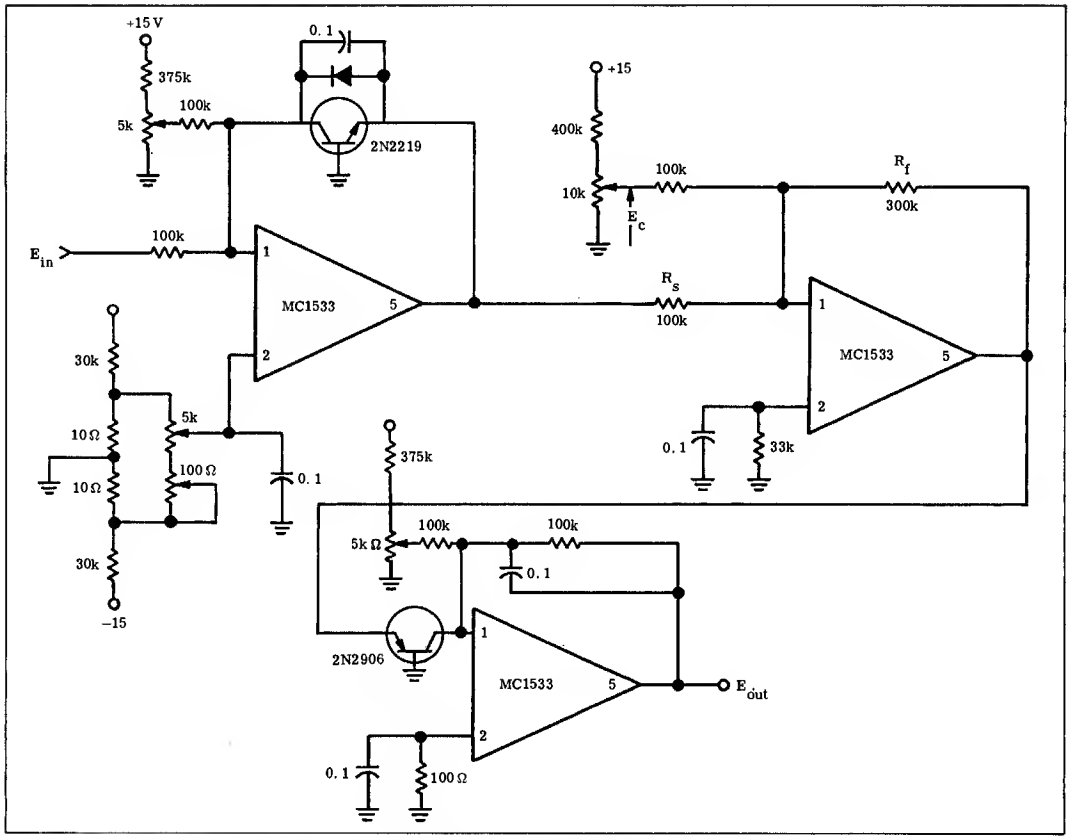


FIGURE 7 — CIRCUIT FOR COMPUTING $Z = X^n$

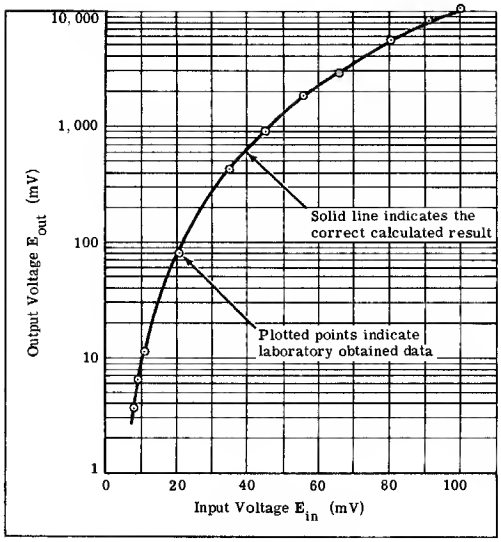


FIGURE 8 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = 2

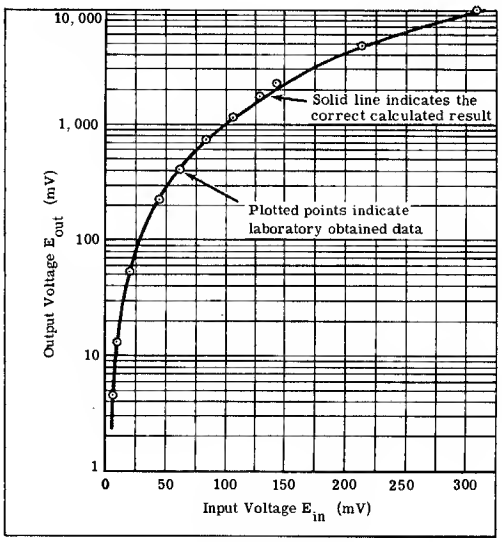


FIGURE 9 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = 3

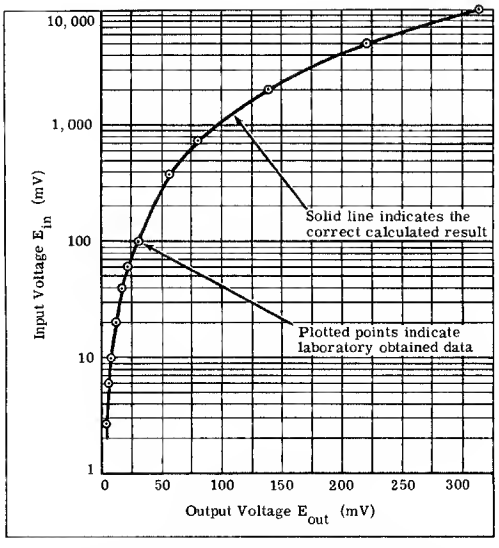


FIGURE 10 — OUTPUT VS. INPUT RESPONSE OF FIGURE 7 FOR a = ½

X Input #1	Y Input #2	Z Output	Calculated Z = XY	Difference	% Error
0.995 mV	13.8 mV	14.0 mV	13.72	0.28	2.04
	81 mV	82.4 mV	80.6	1.8	2.2
	297 mV	308 mV	295.5	12.5	4.2
	605 mV	695 mV	647	48	7.4
	1.042 V	1.110 V	1.038	0.072	6.9
	1.346 V	1.44 V	1.338	0.102	7.7
	2.98 V	2.99 V	2.965	0.025	0.8
	4.99 V	5.04 V	4.97	0.07	1.4
	10.11 V	10.34 V	10.06	0.28	2.8
	12.97 V	12.5 V	12.4	0.1	0.8
4.0 mV	14.44 mV	47.0 mV	57.8	0.8	1.4
	40.9 mV	154.9 mV	163.8	8.9	5.4
	102.3 mV	397 mV	410	13	3.2
	250 mV	1.02 V	1.00	0.02	2.0
	500 mV	2.05 V	2.00	0.05	2.5
	730 mV	3.08 V	2.95	0.13	4 4
	1.003 V	4.28 V	4.02	0.26	6.5
9.8 mV	7.45 mV	72.9 mV	73	0.1	0.14
	14.5 mV	143 mV	142	1	0.7
	40.9 mV	407 mV	401	6	1.5
	85 mV	837 mV	833	4	0.48
	199 mV	2.04 V	1.95	0.09	4.6
	250 mV	2.54 V	2.45	0.09	3.7
50 mV	14 mV	754 mV	700	54	7.7
	50 mV	2.56 V	2.5	0.06	2.4
	102 mV	5.31 V	5.10	0.21	4.1
	155 mV	7.94 V	7.75	0.19	2.5
	207 mV	10.38 V	10.35	0.03	0.29
	250 mV	12.54 V	12.50	0.04	0.32
100.3 mV	5.6 mV	598 mV	562	36	6.4
	14.5 mV	1.44 V	1.455	0.015	1.0
	50 mV	4.91 V	5.02	0.11	2.2
	102 mV	10.2 V	10.23	0.03	0.29
	120 mV	11.87 V	12.04	0.17	1.4
499 mV	5.07 mV	2.48 V	2.53	0.05	2.0
	10.08 mV	5.02 V	5.04	0.02	0.4
	20.15 mV	9.30 V	10.07	0.77	7.7

TABLE I — TABULATED RESULTS FROM MULTIPLIER CIRCUIT Z = XY

APPENDIX

The emitter current of Figure 1 is given by the expression

$$I_E = I_{ES}[e^{qV_E/kT} - 1] - \alpha_I I_{CS}[e^{qV_C/kT} - 1] \qquad (10)$$

where I_{ES} = emitter reverse saturation current
I_{CS} = collector reverse saturation current
α_I = inverted common base current gain

The collector current is given by

$$I_C = I_{CS}[e^{qV_C/kT} - 1] - \alpha_n I_{ES}[e^{qV_E/kT} - 1] \qquad (11)$$

where α_n = normal common base current gain.

Equations (1) and (2) must be modified to include those adverse components such as surface leakage currents and space charge generated currents. Since these currents generally behave as majority carriers in the base region, they are consequently not collected and do not appear at the collector junction. These currents may be included in equations (10) and (11) as follows:

$$I_E = I_{ES}[e^{qV_E/kT} - 1] - \alpha_I I_{CS}[e^{qV_C/kT} - 1] + \Sigma\, I_{ES_i}[e^{qV_E/kTm_i} - 1] \qquad (12)$$

$$I_C = I_{CS}[e^{qV_C/kT} - 1] - \alpha_n I_{ES}[e^{qV_E/kT} - 1] + \Sigma\, I_{CS_j}[e^{qV_C/kTm_j} - 1] \qquad (13)$$

If we now set $V_C = 0$ in equation (13) we find

$$I_C = -\alpha_n I_{ES}[e^{qV_E/kT} - 1] \qquad (14)$$

For $V_E > 100$ mV, equation (14) reduces to

$$I_C = -\alpha_n I_{ES}[e^{qV_E/kT}] \qquad (15)$$

REFERENCES

1. William L. Paterson: Multiplication and Logarithmic Conversion by Operational Amplifier-Transistor Circuits. The Review of Scientific Instruments, Vol. 34, No. 12, Dec. 1963.

2. Leo L. Wisseman: A High Voltage Monolithic Operational Amplifier. Integrated Circuits Application Note, AN-248.

APPLICATIONS OF THE MC1530 -31 INTEGRATED OPERATIONAL AMPLIFIERS

I. INTRODUCTION

The MC1530 and MC1531 operational amplifiers in Figures 1 and 2 are constructed to best utilize the advantages of monolithic integrated circuits. Such advantages as low offset voltage and current, excellent temperature tracking, increased reliability, small size, and reduced cost make the integrated circuits more attractive than many discrete operational amplifiers now in use. On the other hand, many discrete operational amplifiers now in use are of such high quality that their performance cannot presently be equaled by monolithic, high production integrated amplifiers. This condition exists because of the present state-of-the-art of monolithic integrated circuit processing technology. Therefore, a performance cost trade-off must be evaluated when the integrated circuit amplifier is considered for design into any system.

The purpose of this application note is to assist the circuit and system designer in evaluating the performance of the MC1530 and MC1531 amplifiers. This is accomplished by first explaining the detailed A.C. and D.C. operation of each stage in the circuits and some of the constraints on the circuit design that exist because of monolithic fabrication.

After the circuitry and constraints are explained, the amplifiers are applied to four basic operational amplifier applications: a summing amplifier, an integrator, a d.c. comparator, and transfer function simulation. These applications are only representative of the many that could be used, but they indicate that the MC1530 and MC1531 integrated amplifiers are extremely useful low cost tools.

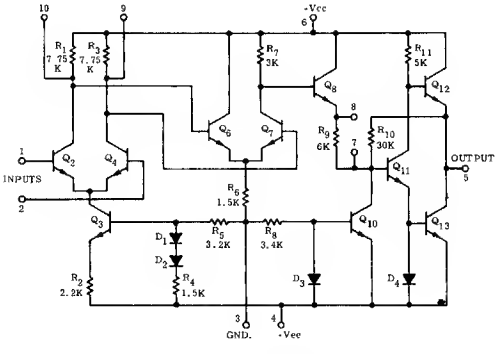


FIGURE 1 — MC1530

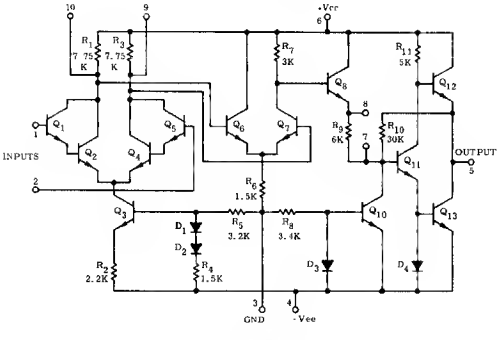


FIGURE 2 — MC1531

II. FABRICATION CONSTRAINTS ON PERFORMANCE

In fabricating an amplifier on a single monolithic chip, the first consideration is the resistivity of the epitaxial layer used for building the components by diffusion processes. Collector-emitter breakdown voltage and collector saturation resistance of transistors are direct functions of the epitaxial resistivity—the higher the resistivity, the higher the breakdown voltage and the higher the collector saturation resistance. High breakdown voltages are desired, while high saturation resistances are undesirable. For the MC1530-31 operational amplifiers, breakdown voltages of 20 volts are achieved while saturation resistances are less than 50 ohms. Therefore, the maximum output voltage swing of 16 volts peak to peak (using ±9 volt supplies) does not approach breakdown in the output devices. At the same time, the collector saturation resistance does not affect the ability to drive loads down to 500 ohms.

In any integrated amplifier, it is very important that critical d.c. levels be a function of resistor ratios and not absolute values. In the MC1530-31, the output d.c. level is a function of only resistor ratios—not of the absolute value of any resistor or of the beta of any device in the circuit. Therefore, the variation of the output voltage with temperature is very small and the major contributor to this variation is any mismatch of the input circuitry. In addition, the open loop gain is very stable: 72 db ± 1.5 db from T = -55°C to T = +125°C.

The ability to match very closely the V_{be} and beta of the input transistors is a strong function of the manner in which these devices are placed on the monolithic chip. By placing these devices very close to each other, the diffusion profiles match each other very closely resulting in very low input offset voltages and currents. In addition, when the devices are very close together thermal gradients across the chip are minimized resulting in excellent tracking with temperature. The MC1530-31 offset voltages of 2 mv and drift of 3.8 $\mu v/^{o}C$ indicates proper layout of the devices on the chip.

Both the MC1530 and MC1531 are fabricated on one monolithic die and the amplifier dies, without wirebonds, are identical. The two circuits, when viewed from their external connections, are distinct from each other because the MC1530 has two internal wire bonds that are not in the MC1531. These two connections convert the Darlington compound circuit used in the MC1531 to a single transistor, resulting in the MC1530 circuit. The two versions offer the circuit designer the option of high gain (5000) and moderate input impedance (10K) or moderate gain (2500) and high input impedance (1 megohm). In addition, the use of two versions with modified input stages requires only two pins for input connections. The biasing, output, and ground leads require four pins, leaving four pins that may be used for internal connections. This allows the popular ten pin TO-5 package to be used and gives the designer a great deal of flexibility in using the four internal points for shaping open loop response, modifying slew rate, noise suppression, etc.

III. CIRCUIT OPERATION

The MC1530 or 31 amplifier can be conveniently considered as a multi-stage amplifier. The MC1530 circuit is redrawn in Figure 3 with dotted lines used to separate the complete circuit into a series of stages. A brief description of the operation and d.c. biasing of each stage in Figure 3 follows:

A. Input Differential Amplifier

Transistors Q_2 and Q_4 differentially amplify the input signal, and Q_3 is a temperature compensated current source used primarily to provide a high common mode rejection.

First considering a.c. operation of the input circuit, the differential voltage gain of the amplifier is given by:

$$A_V \approx \frac{R_L}{r_{e1}} \qquad (1)$$

where R_L = effective load resistance: R_1 or R_3 in parallel with the input impedance of the second stage.

$$r_{e1} \approx \frac{26}{I_e(mA)}$$

(I_e is the emitter current of either Q_2 or Q_4)

For the first stage (as shown later) $I_e \approx 0.5$ mA so that $r_e \approx 52$ ohms. The differential input impedance to the second stage is approximately $2\beta r_{e_2} \approx 5.0$ K ohms; therefore,

$$R_L = \frac{(5K)(7.75K)}{12.75\ K} = 3.02 \text{ K ohms.}$$

From (1) the differential voltage gain of the first stage is:

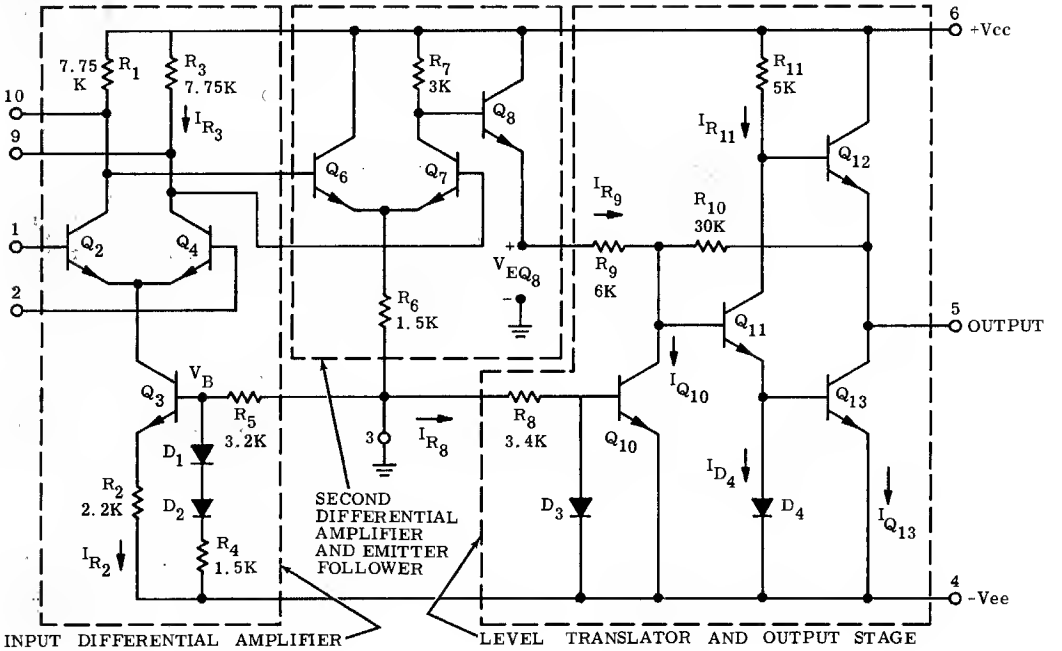
$$A_v \approx \frac{3.02K}{52} \approx 58.5$$

As will be seen later, this is the highest voltage gain stage in the amplifier. A high gain first stage is desirable in order to minimize the effects of V_{be} and β mismatch in the following stages; i.e., any offset in the second differential amplifier is not amplified by the high gain first stage.

The collectors of the first stage are wire bonded to pins 9 and 10 to provide connection points for open loop frequency compensating networks. By using frequency compensation in the first stage of operational amplifiers, the best slew rate* may be obtained. If a single capacitor is used for compensation; it is easily seen that the above statement is true, since voltage variation between the input collectors is smaller at the front than at any other point in the amplifier. Therefore, the time required for the capacitor to reach a fully charged value is minimized. By using this type of compensation a maximum slew rate of 4.5 volts /μ-sec can be obtained from the amplifier when compensated to assure a stable closed loop gain of unity. The MC-1530-31 data sheet shows a curve of slew rate versus the value of capacitance used between pins 9 and 10. Therefore, the circuit designer can first compensate the open loop response to assure closed loop stability and then use the data sheet to determine a typical maximum slew rate.

Before the second stage of the circuit is considered, it is necessary to determine the d.c. voltage from the collectors of the first stage to ground, since these voltages will establish the second stage operating point. In addition, the d.c. voltages from the collector of Q_2 and Q_4 to ground and from the base of Q_3 to ground determine the maximum common mode swing of the amplifier. In all calculations from Figure 3, it is assumed that the base-emitter voltage of transistors and diode forward voltage is approximately 0.7 volts and that base currents are negligible. In addition, the voltages are assumed positive with respect to ground as shown in Figure 3 and the currents in the direction shown.

*Slew rate is defined as the maximum rate of change of output voltage with respect to time: $\frac{\Delta e_o}{\Delta t}$.



NOTES

(1) ALL DIODE FORWARD VOLTAGES AND BASE-EMITTER VOLTAGES ARE APPROXIMATELY 0.7 VOLTS.

(2) ALL BASE CURRENTS ARE NEGLECTED

(3) NOTATION: V_{BQ_3} IS READ AS THE POSITIVE TO NEGATIVE VOLTAGE FROM BASE TO GROUND FOR Q_3; V_{EQ_8} IS FROM THE EMITTER OF Q_8 TO GROUND, ETC.

FIGURE 3

The starting point in biasing the amplifier is the calculation of the current generated by current source Q_3. This may be done by calculating the voltage on the base of Q_3 and using this voltage to determine the current through R_2, which is approximately the value of the current source:

$$V_{BQ_3} \approx \frac{(-Vee + 2\,(0.7))\,R_5}{(R_4 + R_5)} \qquad (2)$$

$$I_{R_2} \approx \frac{Vee + (V_{BQ_3} - 0.7)}{R_2} \qquad (3)$$

For Vee = 6 volts, $V_{BQ_3} \approx -3.14$ V and $I_{R_2} \approx 1.0$ ma.

If it is assumed by a first approximation that the integrated transistors are perfectly matched, one-half the collector current of Q_3 will flow through Q_4 and one-half through Q_2 so that the current through R_3 or R_4 is:

$$I_{R_3} = I_{R_4} = \frac{1}{2R_2}\left[Vee - 0.7 - \frac{(Vee - 1.4)\,R_5}{(R_4 + R_5)}\right] \qquad (4)$$

Finally, the voltage on the base of Q_6 or Q_7 is:

$$V_{BQ_6} = V_{BQ_7} = Vcc - I_{R_3} R_3$$

$$= Vcc - \frac{R_3}{2R_2}\left[Vee - 0.7 - \frac{(Vee - 1.4)\,R_5}{(R_4 + R_5)}\right] \qquad (5)$$

For Vcc = Vee = 6 volts, $V_{BQ_6} = V_{BQ_7} \approx 2.2$ volts.

(Observe that only the magnitude of the power supply voltages are used in all calculations, the sign is taken into account in the above equations.) The calculated values of V_{BQ_3} and V_{BQ_6} or V_{BQ_7} determine the maximum input common mode voltage range. When using ± 6 volt supplys, this range is ± 2 volts maximum.

B. Second Differential Amplifier

The second differential stage provides additional voltage gain ($A_V \approx 20$) and the output is taken from Q_7 (single-ended), through emitter follower Q_8. Since this amplifier will not have an appreciable input common mode swing, the resistor R_6 is used as a current source, and provides adequate common mode rejection. Before proceeding to the third stage, the D.C. voltage at the emitter of Q_3 must be calculated, since this voltage level is essential to the understanding of the level translator and the output stage. The results of this calculation are shown in equation (6); details are omitted but the method is identical to that used in the first stage calculations.

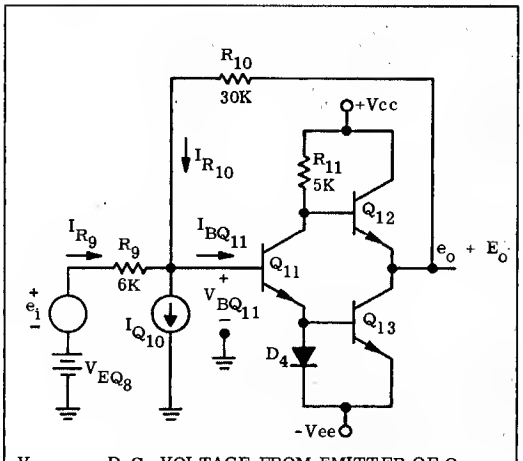
$$V_{EQ_8} = Vcc - \frac{R_7}{2R_6}\left(Vcc - \frac{R_3}{2R_2}\left[Vee - 0.7V - \frac{(Vee - 1.4V)\,R_5}{(R_4 + R_5)}\right] - 0.7\,V\right) - 0.7\,V \qquad (6)$$

For Vee = Vcc = 6 volts, $V_{EQ_8} \approx +3.82$.

C. Level Translator and Output Stage

The problem of level translation arises because of the need for large peak to peak voltage swings at the amplifier output. Since symmetrical a.c. swings are desired the d.c. output voltage should be zero volts; i.e. the amplifier output varies positive and negative about ground. In addition, this voltage should be zero volts so that no current will flow in d.c. coupled loads when the differential input voltage is zero volts. The mismatching of V_{be} and β in the input transistors can cause the d.c. output level to move drastically away from zero volts, and this effect is considered in the next section. However, if the voltage at the emitter of Q_8 (+3.8 volts) is d.c. coupled with gain through the output stage then the output will be between +3.8 volts and the positive supply. Therefore, a d.c. level translation problem exists between the emitter of Q_8 and the output: the +3.8 d.c. voltage must be reduced to zero volts at the output, and the amplifier must be d.c. coupled between the two points.

The circuit of Figure 4 is derived from Figure 3, and will be used to explain the operation of level translation and the output stage. The circuitry in Figure 3 from the emitter of Q_8 to the output may be driven from a voltage source since the impedance seen looking into the emitter of Q_8 is very low. The representation is shown in Figure 4, with e_i representing the a.c. variation at the emitter of Q_8 and V_{EQ_8} the d.c. voltage to ground. In addition, transistor Q_{10} (Figure 3) acts as a d.c. current source and is drawn as such in Figure 4. The value of $I_{Q_{10}}$ may be calculated from Figure 3 as follows:



V_{EQ_8} - D.C. VOLTAGE FROM EMITTER OF Q_8 TO GROUND (+3.8 VOLTS WHEN Vcc = Vee = 6 VOLTS)

e_i - A.C. VOLTAGE GENERATOR

$I_{Q_{10}}$ - D.C. CURRENT SOURCE (COLLECTOR CURRENT OF Q_{10} IN FIGURE 3)

e_o - A.C. OUTPUT VOLTAGE

E_o - D.C. OUTPUT VOLTAGE

$V_{BQ_{11}}$ - D.C. VOLTAGE FROM BASE OF Q_{11} TO GROUND $V_{BQ_{11}} \approx -(Vee - 1.4V)$

FIGURE 4

(1) The current I_{R_8} is given by:

$$I_{R_8} \approx \frac{Vee - 0.7}{R_8}$$

(2) If the diode D_3 matches identically the base emitter junction of Q_{10}, then the emitter current of Q_{10} will be identical to I_{R_8}. Then:

$$I_{Q_{10}} \approx I_{R_8} \approx \frac{Vee - 0.7}{R_8} \qquad (7)$$

and $I_{Q_{10}}$ is a constant current.

From Figure 4, the D.C. output voltage may be derived by assuming $e_i = 0$ and $e_o = 0$:

$$I_{R_9} = \frac{V_{EQ_8} - V_{BQ_{11}}}{R_9} = \frac{V_{EQ_8} + Vee - 1.4}{R_9} \qquad (8)$$

Observe that I_{R_9} is essentially constant since V_{EQ_8} and Vee are constant. Then, summing currents at the base of Q_{11}:

$$I_{R_9} + I_{R_{10}} = I_{Q_{10}} + I_{BQ_{11}} \qquad (9)$$

For purposes of explanation, assume that $I_{BQ_{11}}$ can be neglected. The error caused by neglecting $I_{BQ_{11}}$ will appear in the expression for output voltage. If this error resulted in $e_o = 0.5$ volts D.C. instead of 0 volts, when referred to the input it results in an equivalent input offset voltage of 0.1 mv (for an open loop gain of 5000). This value is insignificant compared to a 0.1 mv V_{be} mismatch on the input transistors since input mismatches are multiplied by the open loop gain. Therefore, (9) reduces to:

$$I_{R_9} + I_{R_{10}} \approx I_{Q_{10}} \qquad (10)$$

From Figure 4:

$$E_o = I_{R_{10}} R_{10} + V_{BQ_{11}} \qquad (11)$$

and

$$V_{BQ_{11}} \approx -(Vee - 1.4V) \qquad (12)$$

Then,

$$E_o \approx (I_{Q_{10}} - I_{R_9}) R_{10} + V_{BQ_{11}} \qquad (13)$$

Substituting equations (7) and (8) into (12) and simplifying:

$$E_o \approx Vee\left(\frac{R_{10}}{R_8} - \frac{R_{10}}{R_9} - 1\right) - V_{EQ_8}\left(\frac{R_{10}}{R_9}\right) + 1.4\left(1 + \frac{R_{10}}{R_9} - \frac{R_{10}}{2R_8}\right) \qquad (14)$$

Observe that the d.c. output level is a function of resistor ratios and not of the absolute value of any resistor. Substituting Vee = 6 volts, $V_{EQ_8} = 3.82$ volts, and the values of resistors shown in Figure 3, into (14):

$$E_o \approx 0.046 \text{ volts}$$

Therefore, the +3.82 volt d.c. level at the emitter of Q_8 has been translated to essentially 0 volts (within the range of approximation: if $V_{EQ_8} = 3.8292$ volts, then $E_O = 0$ volts) by the use of feedback and current summing into a constant current source at the base of transistor Q_{11}.

If $E_O = 0$ volts, the remaining D.C. biasing currents may be calculated:

$$I_{R_{11}} \approx \frac{Vcc - 0.7}{R_{11}}$$

$$I_{R_{11}} \approx 1.06 \text{ ma for Vcc} = 6 \text{ volts}$$

Since the current through diode D_4 is approximately $I_{R_{11}}$, the current through the output transistors may be found. Previously it was stated that if the diode D_4 matched identically the base-emitter junction of Q_{13}, then $I_{Q_{13}} = 1.06$ ma. For the MC-1530-31, the base-emitter junction of Q_{13} is 3 times larger than the area of D_4 so that:

$$I_{Q_{12}} \approx I_{Q_{13}} \approx 3(I_{D_4}) \approx 3.18 \text{ ma}$$

Therefore, the MC-1530 will drive load resistors as low as 1 K to a maximum peak to peak swing of approximately 11 volts.

Using the equivalent circuit of Figure 4, the a.c. voltage gain of the output stage is:

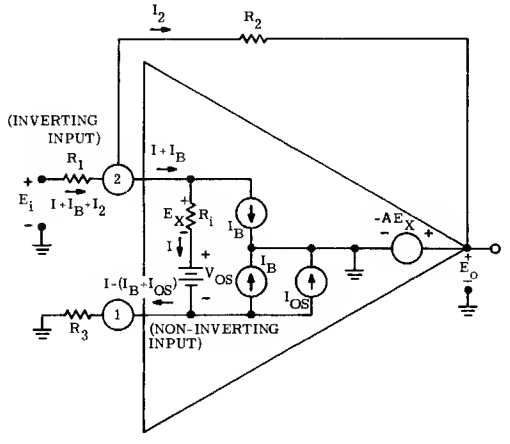
$$A_V \approx \frac{e_o}{e_i} \approx \frac{R_{10}}{R_9} \approx 5$$

(assuming that the input impedance to the base of Q_{11} is very high). Therefore, for an output peak to peak voltage swing of 10 volts (±5), the D.C. levels are adequate throughout the amplifier, and the complete open loop voltage gain is typically 6000.

IV. APPLICATIONS

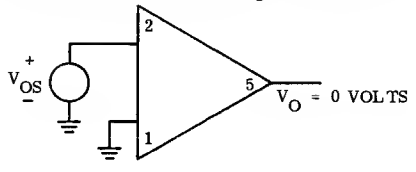
A. D.C. Biasing

In this section, the operational amplifier is considered in terms of the d.c. voltages and currents that can be measured at the input and output terminals. These measurable quantities are shown in an equivalent circuit for the amplifier in Figure 5; and are also defined in the figure. In addition, the general case of resistances, from each input to ground and negative feedback are considered by connecting R_1, R_2, and R_3 as shown.



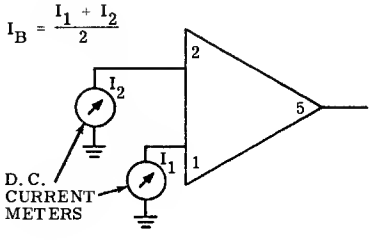
OUTPUT IMPEDANCE $<50\Omega$ AND IS NEGLECTED

V_{OS} = INPUT OFFSET VOLTAGE (VOLTAGE NECESSARY TO CAUSE $V_O = 0$ AS SHOWN)



I_B = AVERAGE INPUT BIAS CURRENT

$$I_B = \frac{I_1 + I_2}{2}$$



I_{OS} = INPUT OFFSET CURRENT = $I_1 - I_2$

A = OPEN LOOP VOLTAGE GAIN = E_o/E_2

R_i = INPUT RESISTANCE

E_i = D.C. INPUT VOLTAGE

E_o = D.C. OUTPUT VOLTAGE

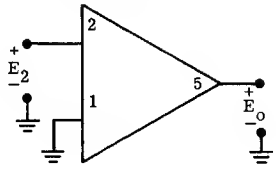


FIGURE 5 – O.C. MODEL FOR OPERATIONAL AMPLIFIER

Using the currents and voltages as shown in Figure 5, the following equations are written:

$$E_i - V_{OS} = (I + I_B + I_2)R_1 + IR_i + \left[I - (I_{OS} + I_B)\right]R_3 \tag{15}$$

$$-E_o + V_{OS} = -\left[I - (I_B + I_{OS})\right]R_3 - IR_i + I_2R_2 \tag{16}$$

In addition, from the model:

$$I = \frac{E_x}{R_i} = -\frac{E_o}{AR_i} \tag{17}$$

Solving for I_2 from (16) and substituting the result and equation (17) into (15) the equation for output voltage is:

$$E_o = \frac{-KE_i + V_{OS}(K+1) + KI_BR_1 - (K+1)(I_B + I_{OS})R_3}{1 + \frac{K}{A}\left[\frac{1}{R_i}\left(R_1 + R_3\left[\frac{K+1}{K}\right]\right) + \left[\frac{K+1}{K}\right]\right]} \tag{18}$$

where $K = R_2/R_1$.

The K term in (18) represents the closed loop voltage gain if the amplifier was ideal. The term:

$$V_{OS}(K+1) + KI_BR_1 - (K+1)(I_B + I_{OS})R_3 \tag{19}$$

is the d.c. error at the output caused by offset voltages and currents and bias current, while the term:

$$\frac{K}{A}\left[\frac{1}{R_i}\left(R_1 + R_3\left[\frac{K+1}{K}\right]\right) + \left[\frac{K+1}{K}\right]\right] \tag{20}$$

is the error caused by $R_i \neq \infty$ and $A \neq \infty$.

The results in equations (18), (19), and (20) can be extended to the a.c. case when e_i = a.c. input voltage and the resistances are replaced by impedances. Care must be taken, however, to prevent <u>both</u> Z_1 and Z_2 from becoming infinite at d.c. (a.c. coupling) since base current I_B will then be blocked to one side of the amplifier. In extending the analysis to a.c. the following equation is obtained:

$$e_o(S) = \frac{-K(S)\,e_i(S)}{1 + \frac{K}{A}(S)\left[\frac{1}{Z_i}\left(Z_1(S) + Z_3(S)\left[\frac{K(S)+1}{K(S)}\right]\right) + \frac{K(S)+1}{K(S)}\right]}$$

$$+ \frac{V_{OS}(K(0)+1) + K(0)I_BZ_1(0) - (K(0)+1)(I_B+I_{OS})Z_3(0)}{\frac{K}{A}(0)\left[\frac{1}{R_i}\left(Z_1(0) + Z_3(0)\left[\frac{K(0)+1}{K(0)}\right]\right) + \frac{K(0)+1}{K(0)}\right]} \tag{21}$$

where $S = \sigma + jw$ (complex frequency) or $S = jw$ for steady state calculations and $K(S) = Z_2(S)/Z_1(S)$ and $K(0) = Z_2(0)/Z_1(0)$.

Equation (21) concisely gives: the a.c. closed loop voltage gain K(S) for the ideal case, the error as a function of frequency in the denominator, and the output offset voltage caused by the d.c. value of the impedances Z_1, Z_2, and Z_3 divided by the d.c. error. The numerator of the latter term is very useful:

$$\text{D.C. output offset} = V_{OS}\,(K(0)+1) + K(0)1_B Z_1(0) - (K(0)+1)\,(1_B + I_{OS})\,Z_3(0) \qquad (22)$$

and will be used later in this report for several calculations.

B. Open Loop Frequency Compensation

As previously explained, four internal points in the amplifier are wire bonded to external pins 7, 8, 9, and 10 for frequency compensation. The criterion for unconditional stability when resistive negative feedback is used is that the open loop voltage gain must have a 6db/octave slope when passing through 0 db. When using the MC-1530-31, if no external capacitors are connected to pins 7, 8, 9, or 10 the amplifier does not oscillate without feedback. However, as shown by the uncompensated open loop gain slope on the data sheet, it is virtually impossible to close the loop and keep the amplifier stable. Therefore, consider first the use of pins 9 and 10 for open loop frequency compensation.

As previously shown, the differential gain of the first stage with a capacitor C between pins 9 and 10 is:

$$A_{V_1} \approx \frac{Z_L}{r_{e1}} \qquad (23)$$

Figure 6 shows the representation of Z_L when a capacitor is used:

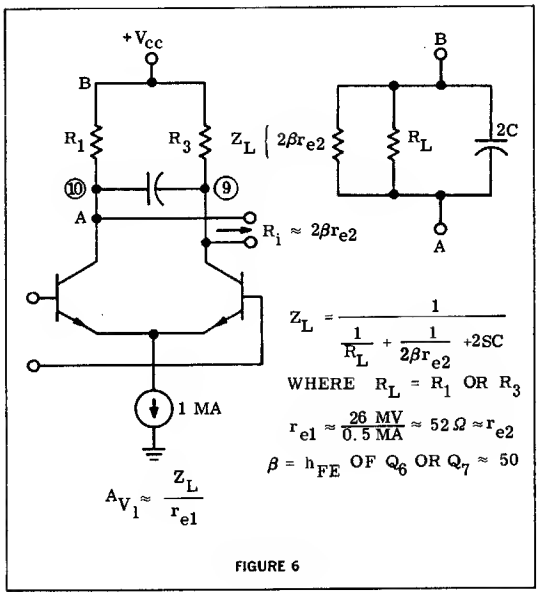


FIGURE 6

$$Z_L = \frac{1}{\frac{1}{R_1} + \frac{1}{2\beta r_{e2}} + 2SC} \qquad (24)$$

Substituting (24) into (23) and simplifying:

$$A_{V_1}(S) \approx \frac{1}{2r_{e1}C}\left[\frac{1}{S + \frac{(R_L + 2\beta r_{e2})}{4\beta R_L r_{e2} C}}\right] \qquad (25)$$

Since the gain equation for the first stage is to determine the frequency response, the complete expression for the open loop gain is:

$$A_{VOL} = A_{V_1}(S)A_{V_2}A_{V_3} \approx 100\ A_{V_1}(S)$$

since

$$A_{V_2} \approx 20 \text{ and } A_{V_3} \approx 5$$

or,

$$A_V(S) \approx \frac{50}{r_{e1}C}\left[\frac{1}{S + \frac{(R_1 + 2\beta r_{e2})}{4\beta R_1 r_{e2} C}}\right] \qquad (26)$$

The d.c. value of the open loop gain is:

$$A_V(0) \approx \frac{100}{r_{e1}}\left[\frac{2\beta R_1 r_{e2}}{R_1 + 2\beta r_{e2}}\right] \approx 6000 \qquad (27)$$

which checks with previous calculations and the typical value on the MC-1530 data sheet. The -3 db value of $A_V(S)$ can be used to find the 3 db frequency using (26) and (27). At $\omega = \omega_{3db}$ $A_V(\omega_{3db}) = 0.707\ A\ (0)$, so that

$$0.707\left[\frac{100}{r_{e1}}\left[\frac{2\beta R_1 r_{e2}}{R_1 + 2\beta r_{e2}}\right]\right] = \frac{50}{r_{e1}C}\left[\frac{1}{j\omega_{3db} + \left[\frac{R_1 + 2\beta r_{e2}}{4\beta R_1 r_{e2} C}\right]}\right] \qquad (28)$$

Simplifying and solving for ω_{3db}:

$$\omega_{3db} = \sqrt{\frac{1}{(4.24 \times 10^3)C}\left[\frac{R_1 + 2\beta r_{e2}}{4\beta R_1 r_{e2} C}\right] - \left[\frac{R_1 + 2\beta r_{e2}}{4\beta R_1 r_{e2} C}\right]^2} \qquad (29)$$

Using $\beta \approx 50$, $r_{e_2} \approx 50$, $R_1 = 7.75$ K, and Vcc = Vee = 6 volts:

$$\omega_{3db} \approx \frac{1.09 \times 10^{-4}}{C} \qquad (30)$$

One method of using the above equations to compensate the amplifier is to first specify the frequency at which $|A_V(\omega)| = 0$ db. For the MC-1530 amplifier, the uncompensated response shown on the data sheet indicates a pole at 1 mc. This pole could arise because of a collector-substrate parasitic, or from the parasitic capacitance of a diffused resistor. Therefore, the open loop compensated gain can be specified to go through 0 db at 1 mc so that this pole can be avoided. From (26):

$$\left|A_V(\omega)\right| = \frac{50}{\omega r_{e1} C} \qquad (31)$$

when,

$$\omega >> \frac{R_1 + 2\ r_{e2}}{4\ R_1 r_{e2} C}$$

For $\left|A_V(\omega)\right| = 1.0$ at $\omega = 2\pi(1 \times 10^6)$ and $re_1 \approx 50\Omega$,

$$C \approx \frac{50}{50(2\pi)(10^6)} \approx 0.16\ \mu f$$

Using a standard value of capacitance C = 0.1 μf, the gain-crossover point from (28) is:

$$f = \frac{50}{(50)(2\pi)(0.1 \times 10^{-6})} = 1.6\ \text{mcs}$$

The 3 db break frequency may be calculated from (27), with C = 0.1 μf:

$$f_{3db} \approx \frac{1}{2\pi}\left(\frac{1.09 \times 10^{-4}}{1 \times 10^{-7}}\right) \approx 174\ \text{cps}$$

As seen on the MC-1530 data sheet, the 0.1 μf capacitor causes the gain to pass through 0 db at 1.4 mcs with $f_{3db} \approx 230$ cps. Therefore, the above equations can be used as a very good approximation to predict the frequency response.

When the MC-1531 amplifier is used, a good approximation to the open loop compensated gain is simply to divide the MC-1530 gain expression by 2:

$$A_{V_{0L}}(S) = \frac{25}{r_{e1} C}\left[\frac{1}{S + \frac{(R_1 + 2\ r_{e2})}{4\beta R_1 r_{e2} C}}\right] \qquad (32)$$

Therefore, the 3 db frequency expressions previously derived will also be approximately divided by 2 when the same value of C is used in the MC-1531.

As pointed out earlier, the best slew rate may be obtained by compensating the amplifier at pins 9 and 10. However, it sometimes becomes necessary to use a lead network to compensate the open loop gain. The points at pins 7 and 8 are provided for this purpose, as shown in the block diagram of Figure 7. From Figure 7:

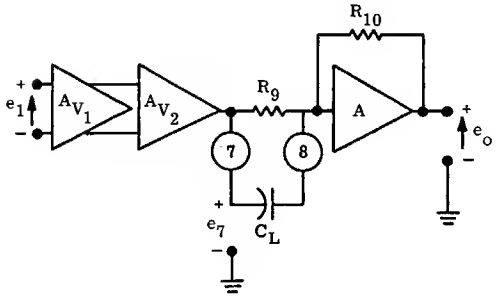


FIGURE 7

$$\frac{e_o}{e_1} = \frac{e_o}{e_7}\frac{e_7}{e_1} \approx A_{V_1} A_{V_2} \frac{e_o}{e_7}$$

where

$$\frac{e_o}{e_7} \approx \frac{R_{10}}{R_9}\ (SR_9C_L + 1)$$

So that the open loop voltage gain can be lead compensated:

$$A_{V_{0L}} \approx A_{V_1} A_{V_2}\left(\frac{R_{10}}{R_9}\left[SR_9C_L + 1\right]\right) \qquad (33)$$

By using all four frequency compensation points, there are many combinations and impedances that may be used to compensate the amplifier. Lead-lag compensation is accomplished by using both of the methods previously discussed at the same time. Another method of compensation that is extremely useful is the use of a capacitor from the output (pin 5) to ground and a capacitor from output to the base of Q_{11} (pin 7). This configuration is used on the MC-1530/31 data sheet primarily for suppression of internally generated broad-band noise voltages. The rms noise voltage at the output can be reduced to 100 uv using this compensating technique, but care must be taken with lead lengths on the external capacitors to avoid oscillations at high frequencies.

C. Specific Applications

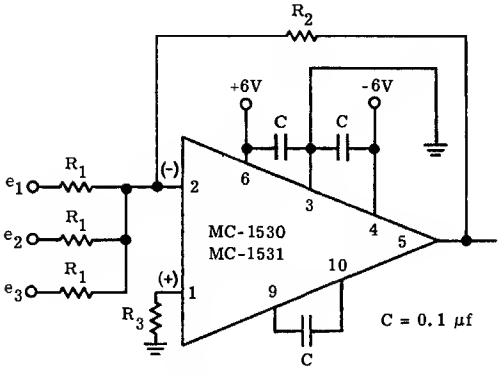


FIGURE 8 -- SUMMING AMPLIFIER

1. Summing Amplifier

The MC-1530 or 31 is connected as a summing amplifier as shown in Figure 8. The input resistors used for summing are equal so that the ideal gain is:

$$e_o = \frac{R_2}{R_1}(e_1 + e_2 + e_3) \qquad (34)$$

Using equations (19) and (20), the d.c. summing errors may be calculated, but R_1 must be modified in the following manner. If $E_i = 0$ in Figure 5, the d.c. offset is that shown by equation (19). However, in Figure 8 three resistors are used instead of one so that:

$$R_1 \text{ equivalent} = \frac{R_1}{3}$$

Then the d.c. offset error (V_E) is:

$$V_E = V_{OS}(K' + 1) + I_B\left[R_2 - (K' + 1)R_3\right] - (K' + 1)I_{OS}R_3 \quad (35)$$

where

$$K' = \frac{3R_2}{R_1}$$

Using (35), R_3 may be selected to set the error due to bias current I_b equal to zero:

$$I_B\left[R_2 - (K' + 1)R_3\right] = 0$$

or

$$R_3 = \frac{R_2}{K' + 1} = \frac{R_2R_1}{3R_2 + R_1} \quad (36)$$

then

$$V_E = V_{OS}(K' + 1) - I_{OS}R_2 \quad (37)$$

The error due to $A_{VO} \neq \infty$ and $R_i \neq \infty$ (E) is:

$$E = \frac{K'}{A_{VOL}}\left[\frac{1}{R_i}\left(R_1 + R_3\left[\frac{K' + 1}{K'}\right]\right) + \frac{K' + 1}{K'}\right] \quad (38)$$

Proceeding with the design of the summing amplifier, assume that the desired output is:

$$e_o = e_1 + e_2 + e_3$$

If $R_1 = R_2 = 10K$, then the ideal amplifier output voltage would be:

$$e_o = (e_1 + e_2 + e_3)$$

From (36),

$$R_3 = \frac{(10K)(10K)}{(30K) + (10K)} = 2.5K$$

From (37), the calculated d.c. offset voltage using typical MC-1530 data sheet values for V_{OS} and I_{OS} is:

$$V_E = (1 \times 10^{-3}) + -(2 \times 15^{7})(1 \times 10^{4}) = 2\ mv$$

(V_E = -12mv for the MC-1531 with a typical V_{OS} = -3mv).

The calculated error due to imperfections is less than 1% and is neglected. Measured data on the MC-1530 and MC-1531 is shown in Table I, and compares very favorably with the calculated values.

Using the compensating scheme of Figure 8, the summing amplifier may be used to accurately sum a.c. voltages up to the closed loop band width of approximately 1 mc. A maximum output swing of 10 volts peak to peak may be obtained up to 1 KC (see data sheet for output swing vs frequency).

TABLE I.

$R_1 = R_2 = 10K\ (\pm 1\%)$ $R_3 = 2.5K\ (\pm 1\%)$

	MC-1530	MC-1531
Offset Voltage ($e_1 = e_2 = e_3 = 0$)	+2 MV	-15 MV
$e_o(e_1 = e_2 = 1V; e_2 = e_3 = 0V)$	-0.9985 V	-1.015 V
$e_o(e_1 = e_2 = 1V; e_3 = 0V)$	-1.9990 V	-2.0163 V
$e_o(e_1 = e_2 = e_3 = 1V)$	-2.9983 V	-3.014 V

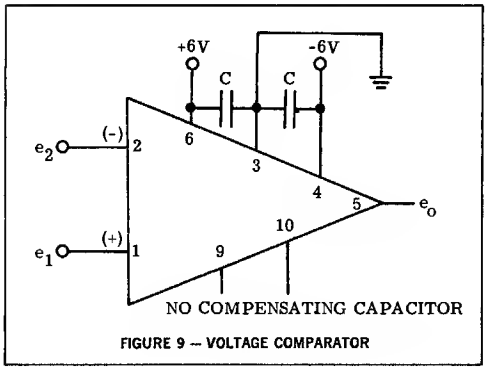


FIGURE 9 -- VOLTAGE COMPARATOR

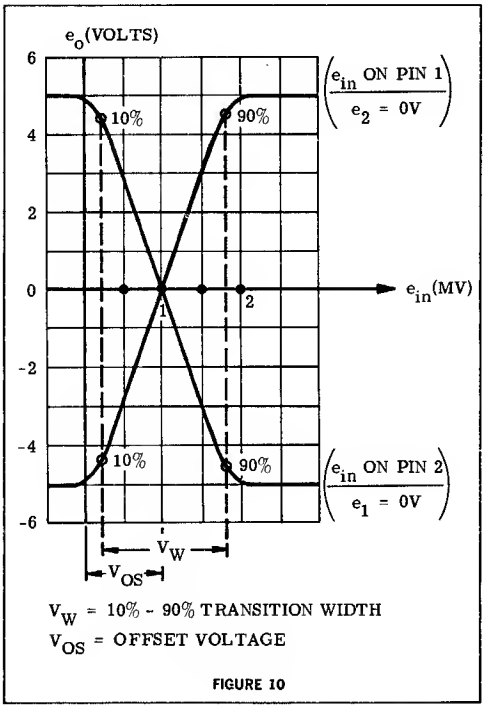


FIGURE 10

2. Voltage Comparator

The MC-1530-31 may be used as a voltage comparator as shown in Figure 9. The input output transfer characteristics of the device is shown in Figure 10, and the voltages of interest are defined for the case where either pin 1 or pin 2 is grounded and the input voltage is applied to the other pin. Observe from Figure 9 that the MC-1530 or 31 can be used without rolloff capacitors; i.e., the amplifier is open loop stable without compensation. The circuit of Figure 9 compares the input voltage with zero volts, but could be used to compare an input voltage e_i with a reference voltage other than ground. However, the reference voltage cannot exceed ±2 volts (the maximum common mode range of the amplifier). Typical values for the offset and transition voltages are:

$$V_{OS} = 1 \text{ mv}$$

$$V_W = 1.8 \text{ mv}$$

Since voltage comparators are usually used to sense the difference between a pulse waveform and a reference voltage, switching times become important. The circuit of Figure 11 was used to measure the switching characteristics of the MC-1530 with a 10-1 overdrive at the input. The storage time is essentially caused by saturation occurring in the latter stages of the amplifier, while the fall time is essentially controlled by the parasitic capacitance in the input stages.

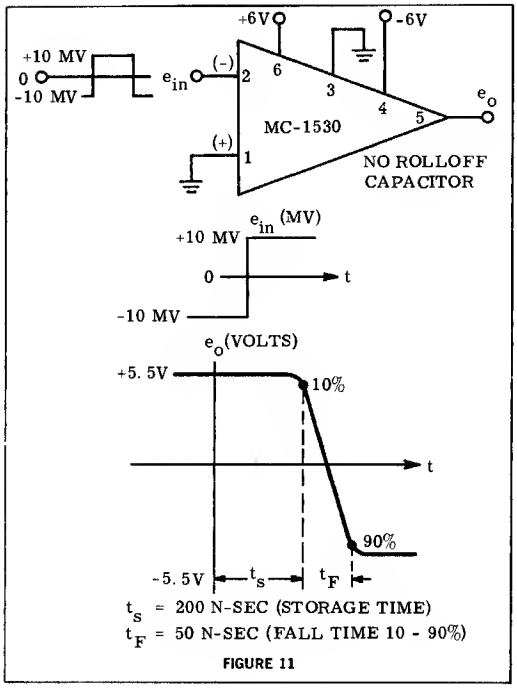


FIGURE 11

Another application for comparators that is often needed in servomechanism work, analog simulation, or as a Schmidtt trigger is shown in Figure 12. The transfer characteristic of the amplifier (Figure 12) shows the hysteresis that results from using R_1 and R_2 in a positive feedback connection. Due to the positive feedback, the transition width, V_W, approaches zero; i.e., the transition width is not a function of the time required for the transition. This time is limited by the maximum slew rate of the amplifier (4.5 V/μ-sec for Figure 12). The threshold voltage (V_T) can be computed from the model of Figure 5, but if $I_B << I_1$ in Figure 12, then:

$$V_T \approx |E_o| \max\left(\frac{R_1}{R_1 + R_2}\right) + V_{OS} \qquad (39)$$

The performance of the circuit in Figure 12 is summarized in Table II.

TABLE II.

	MC-1530	MC-1531
R_1	10 ohms	10 ohms
R_2	10 K	10 K
Transition Width	0	0
Threshold Voltage	+3.8 mv -4.95 mv	-7.0 mv -0.5 mv

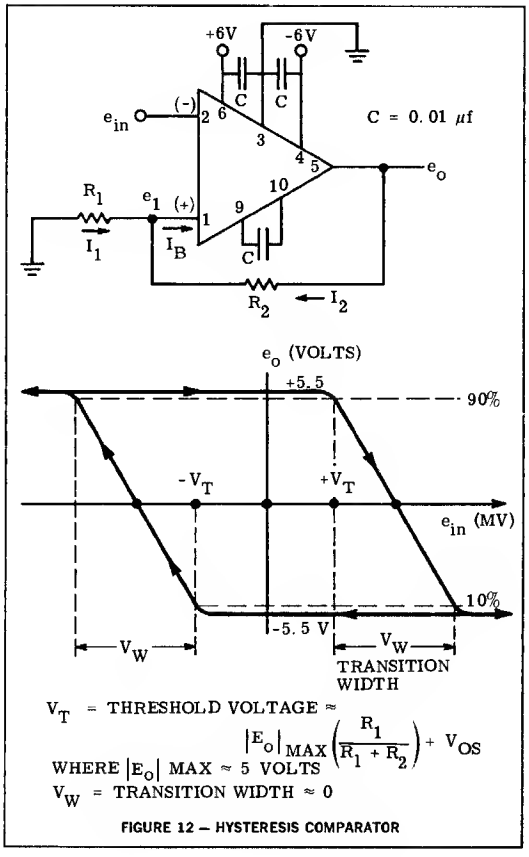


FIGURE 12 — HYSTERESIS COMPARATOR

3. Integration With The MC-1530/31

The MC-1530-31 is connected as an integrator in Figure 13. The biasing network used for this application is designed to minimize the offset voltage drift since this is an error in the integration. Calculating the a.c. closed loop voltage gain of Figure 13:

$$A_V \approx -\frac{Z_f}{Z_1} \qquad (40)$$

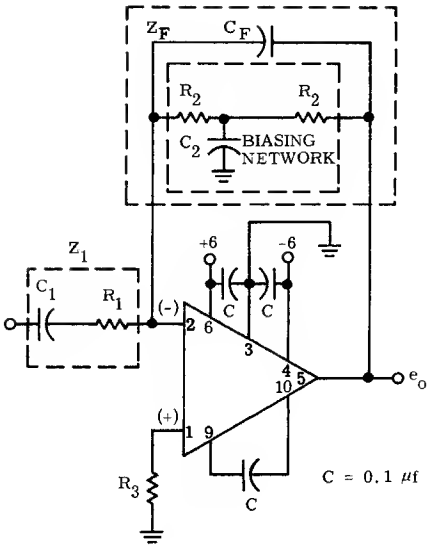


FIGURE 13 — INTEGRATOR CIRCUIT

The exact expressions for Z_f and Z_1 must first be examined to assure that the gain function is of the form:

$$(A_V) = -\frac{1}{SRC}$$

Considering Z_1 first:

$$Z_1 = \frac{SR_1C_1 + 1}{SC_1} \tag{41}$$

Then, for

$$SR_1C_1 >> 1$$

$$Z_1(S) = R_1 \tag{42}$$

which restricts the range of frequencies to

$$\omega >> \frac{1}{R_1C_1} \tag{43}$$

The feedback admittance $1/Z_f$ is given by:

$$\frac{1}{Z_F} = SC_F + \frac{1}{R_2}\left(\frac{S + \frac{1}{R_2C_2}}{S + \frac{2}{R_2C_2}}\right) \tag{44}$$

If

$$S >> \frac{2}{R_2C_2} >> \frac{1}{R_2C_2}$$

Then (44) reduces to

$$\frac{1}{Z_F} = SC_F + \frac{1}{R_2} \tag{45}$$

for

$$\omega >> \frac{2}{R_2C_2}$$

Consider now the d.c. conditions on the integrator. Since the amplifier is a.c. coupled at the input, $Z_1(0) \rightarrow \infty$. Using this fact and equation (22), the output offset voltage is given by:

$$V_{ODC} = V_{OS} + I_B\left[Z_2(0) - Z_3(0)\right] - 1_{OS}R_3 \tag{46}$$

Since $Z_2(0) = 2R_2$, and $Z_3(0) = R_3$, and letting $R_3 = 2R_2$, equation (46) reduces to:

$$V_{ODC} = V_{OS} - 2I_{OS}R_2 \tag{47}$$

Equation (47) reveals two advantages in using a. c. coupling at the input:

(1) The input offset voltage V_{OS} appears directly at the output, i.e., it is not multiplied by the closed loop gain of the amplifier. Therefore, this output contribution is typically 3 mv for the MC-1531 and 1 mv for the MC-1530.

(2) The input offset current is so low (25 ma maximum for the MC-1531) that high impedance levels may be used in the feedback loop with low d.c. offset. If R_2 = 100K, then $2I_{OS}R_2$ = 5 mv.

Therefore, use of a.c. coupling and equal d.c. resistances in the feedback loop and from the non-inverting base to ground will degrade the maximum linear output swing of the MC-1531 by only 8 mv. In addition, the use of a high value for R_2 reduces equation (45) to

$$\frac{1}{Z_f} = SC_f \tag{48}$$

for

$$\omega >> \frac{1}{R_2C_f}$$

Substituting equations (48) and (42) into (40)

$$A_V(S) = -\frac{1}{SR_1C_F} \tag{49}$$

or

$$e_o(t) = -\frac{1}{R_1C_F}\int_0^t e_i(t)\,dt \tag{50}$$

Using the previously developed equations, the frequency range of the integrator must be restricted. First choosing a low frequency for the R_2C_2 time constant; if C_2 = 200 μf, then,

$$\omega_1 >> \frac{2}{(1 \times 10^5)(2 \times 10^{-4})} >> 0.5 \text{ rps}$$

from the restriction on equation (45). If the magnitude of $A_V(\omega)$ is specified at a given frequency, the constant of integration may be found:

Let

$$\left|A_V(\omega)\right| = 10 \text{ (20 db)}$$

at

$$\omega = 2\pi(5\text{KC})$$

Then, from (49):

$$\frac{1}{\omega R_1 C_F} = 10$$

or

$$\frac{1}{R_1 C_F} = 10(2\pi)(5 \times 10^3) \qquad (51)$$

Equation (43) indicates that R_1 should be kept reasonably high so that the frequency range will not be too restricted. Therefore, let R_1 = 10K and from (51) C_f = 318 pf. Choosing a practical value:

$$C_f = 300 \text{ pf.}$$

To complete the design, the input R_1C_1 time constant is chosen for

$$\omega >> 2\pi(400 \text{ cps}) >> \frac{1}{R_1 C_1}$$

and C_1 is calculated:

$$C_1 = 100\ \mu\text{f}$$

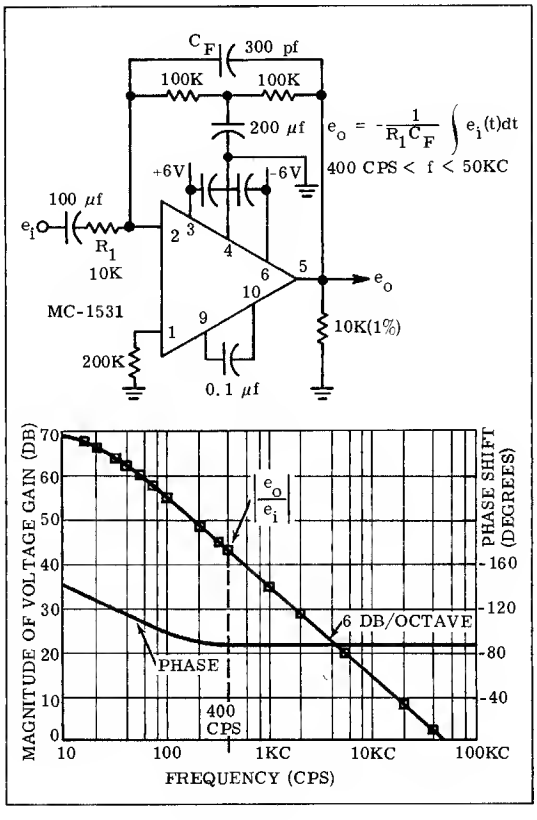


FIGURE 14 — MC1531 INTEGRATOR

The measured response of the integrator constructed with calculated values is shown in Figure 14, and performs as predicted between 400 cps and 50 KC.

4. Simulation of Transfer Functions

The MC-1531 amplifier may be very effectively used in both R-C filters and in transfer function simulation. Using the closed loop gain expression from Figure 13

$$A_{C_L} \approx -\frac{Z_F}{Z_1} \qquad (52)$$

a large number of transfer functions may be generated. As a representative example, the amplifier will be used to simulate equation (53)

$$A_{C_L} = \frac{SRC\,(ST_3 + 1)}{(ST_1 + 1)(ST_2 + 1)^2} \qquad (53)$$

where

$$T_1 = \frac{1}{2\pi(8\text{KC})} = 1.99 \times 10^{-5}$$

$$T_2 = \frac{1}{2\pi(12\text{KC})} = 1.38 \times 10^{-5}$$

$$T_3 = \frac{1}{2\pi(40\text{KC})} = 0.3981 \times 10^{-5}$$

and

$$A_{C_L} = 0 \text{ db at } 10\text{KC}$$

The closed loop expression of equation (53) must first be examined at S = 0 (at d.c.). The MC-1531 should have a very small d.c. offset voltage at the output to obtain the maximum undistorted a.c. output voltage variation. From equation (53), the d.c. closed loop gain is zero. This means that the d.c. value of Z_1 approaches infinity or the d.c. value of Z_f = 0. The Z_f = 0 case requires an undesirable inductor in the feedback loop; so to avoid this case, a.c. coupling may be used at the input which makes $Z_1(0) \rightarrow$ infinity. Then the output offset voltage is the same as that discussed in the integrator:

$$V_{ODC} = V_{OS} + I_B(R_2 - R_3) - I_{OS}R_3$$

If $R_2 = R_3$, then:

$$V_{ODC} = V_{OS} - I_{OS}R_3$$

and the same advantages as those discussed with the integrator apply.

The next step is to synthesize equation (53), then the known value of R_3 may be used to check the output level to make sure that an adequate linear output swing may be obtained from the amplifier. Using equation (52) and tables of R-C transfer impedances found in reference one, equation (53) may be generated. Let $Z_1(S)$ be represented as in Figure 15

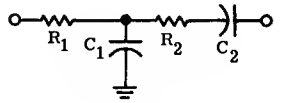
$$Z_1(S) = \frac{(ST_1 + 1)(ST_2 + 1)}{SC_2} \qquad T_1 \neq T_2 \qquad (54)$$

The design equations for the circuit in Figure 15 are:

$$R_1 = \frac{(\sqrt{T_1} - \sqrt{T_2})^2}{C_2} \qquad (55)$$

$$R_2 = \frac{\sqrt{T_1 T_2}}{C_2} \qquad (56)$$

$$C_1 = \frac{\sqrt{T_1 T_2}}{(\sqrt{T_1} - \sqrt{T_2})^2} C_2 \qquad (57)$$

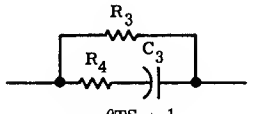


$$Z_1(S) = \frac{(ST_1 + 1)(ST_2 + 1)}{SC} \qquad T_1 \neq T_2$$

FIGURE 15

Next, let Z_f be represented as shown in Figure 16:

$$Z_F(S) = R_3\left(\frac{\theta T_S + 1}{T_S + 1}\right) \qquad \theta < 1$$



$$Z_F(S) = R_3 \frac{\theta TS + 1}{TS + 1} \qquad \theta < 1$$

FIGURE 16

The design equations for the circuit of Figure 16 are:

$$T = (R_3 + R_4) C_3 \qquad (58)$$

$$\theta = \frac{R_4}{R_3 + R_4} \qquad (59)$$

If $T = T_2$ and $\theta T_2 = T_3$, then the closed loop gain expression for Figure 17 is given by:

$$A_{C_L} = \frac{e_o}{e_i} - \frac{Z_F}{Z_1}(S) = -\frac{SR_3C_2(T_3S + 1)}{(ST_1 + 1)(ST_2 + 1)^2} \qquad (60)$$

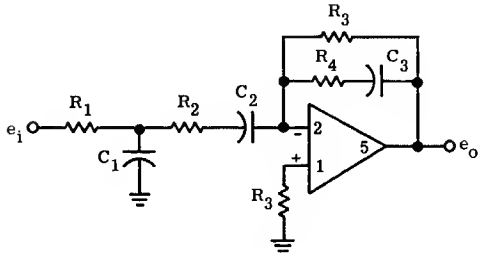


FIGURE 17

Using the time constants T_2 and T_3, θ may be found:

$$\theta = \frac{T_3}{T_2} = \frac{2\pi(12KC)}{2\pi(40KC)} = 0.3$$

There are many ways in which the design equations (55) through (59) may be used to find the R-C values in Figure 17. However, since it is usually required to drive the amplifier from a voltage source, the impedance levels should be high. With this in mind, the design can begin with an arbitrary specification of R_1. Most audio signal generators have 600 ohm internal impedance so that if an arrangement as shown in Figure 18 is used, R_1 should be approximately 10 times larger than R_S (Figure 18) to avoid loading the source. In addition, R_1 should be large enough so that another operational amplifier can drive the circuit of Figure 17 without loading the driving amplifier, thus reducing its output swing. Therefore, let R_1 = 2K; then from equation (55):

$$R_1C_2 = (\sqrt{T_1} - \sqrt{T_2})^2 = 6.73 \times 10^{-7}$$

or

$$C_2 = \frac{6.73 \times 10^{-7}}{2 \times 10^3} = 336 \text{ pf}$$

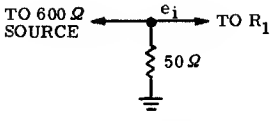


FIGURE 18

Using the value of C_2 and equations (56) and (57), R_2 and C_1 may be calculated, completing the design of Z_1:

$$R_2 = \frac{\sqrt{T_1T_2}}{C^2} = \frac{1.625 \times 10^{-5}}{3.36 \times 10^{-10}} = 48.4 \text{ K ohms}$$

$$C_1 = \frac{\sqrt{T_1T_2}}{(\sqrt{T_1} - \sqrt{T_2})^2} C_2$$

$$C_1 = \frac{(3.36 \times 10^{-10})(1.625 \times 10^{-5})}{6.73 \times 10^{-7}} = 0.0081 \ \mu f$$

To design the feedback impedance Z_f, the closed loop gain expression in equation (60) and the specification that A_{CL} = 0 db at 10 KC are used to calculate R_3. When R_3 is known, equations (58) and (59) may be used to calculate R_4 and C_3.

$$A_{C_L} = \frac{j\omega R_3C_2\left[1 + j\omega(0.398 \times 10^{-5})\right]}{\left[1 + j\omega(1.99 \times 10^{-5})\quad 1 + j\omega(1.38 \times 10^{-5})\right]^2}$$

$$\left|A_{C_L}\right| = 1.0 \text{ and } \omega = 2\pi(1 \times 10^4)$$

then

$$R_3C_2 = 4.16 \times 10^{-5}$$

$$R_3 = \frac{4.16 \times 10^{-5}}{3.36 \times 10^{-10}} = 123.8 \text{ K ohms}$$

from (59)

$$R_4 = \frac{\theta}{(1 - \theta)} R_3$$

$$R_4 = \frac{0.3}{0.7} (123 \text{ K}) = 53 \text{ K}$$

from (58)

$$(R_3 + R_4) C_3 = T = T_2 = 1.38 \times 10^{-5}$$

or

$$C_3 = \frac{1.38 \times 10^{-5}}{1.768 \times 10^{5}} = 75 \text{ pf}$$

The circuit simulating equation (53) is shown in Figure 19 with curves of measured data and data calculated from equation (60).

In using the MC-1530 series to design R-C filters, the same procedure outlined above may be used. However, in the design of filters to meet specified gain, bandwidth, and skirt selectivity, an additional problem arises in approximating the desired frequency response by a transfer function in the S-plane. Several methods are available for solving the approximation problem (one of the best is found in chapter 6 of reference two), but they are beyond the scope of this report.

V. SUMMARY AND CONCLUSIONS

Several circuit design constraints on integrated operational amplifiers caused by monolithic fabrication have been considered. Although all the problems associated with this topic have not been discussed, the major ones of importance are included:

(1) effects of epitaxial resistivity,

(2) importance of resistor ratios, and

(3) importance of transistor and diode matching.

The operation of each stage in the MC-1530-31 is explained and analyzed at d.c. and low frequencies. This clarifies the circuit design and points out the contribution of each stage to the overall amplifier.

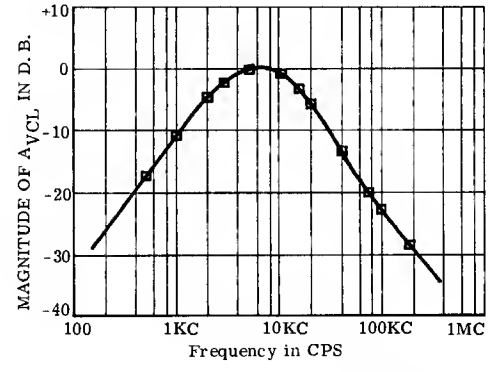
In the final section, as a prelude to practical applications, the details of d.c. biasing and methods of frequency compensation are explained. The note is closed with the design of four practical circuits using the amplifier: a summing amplifier, a voltage compensator, an integrator, and transfer function simulation.

By comparing the measured data with calculated data in the applications section, it is obvious that the MC-1530-31 amplifiers are predictable and useful tools. Since these amplifiers are fabricated by the high volume monolithic process resulting in a low cost, most users should consider them for a wide variety of applications.

VI. REFERENCES

(1) H. Chestnut and R. Mayer "Servomechanisms and Regulating System Design", John Wiley and Sons, Inc., New York, New York, pp 560-571, 1961.

(2) J.G. Truxal "Control System Synthesis", Mc Graw Hill Book Co., Inc., New York, New York, Chapter 6, 1955.



— CALCULATED FROM $A_{VCL} = \frac{SR_3C_2 (ST_3 + 1)}{(ST_1 + 1)(ST_2 + 1)^2}$

□ MEASURED POINTS

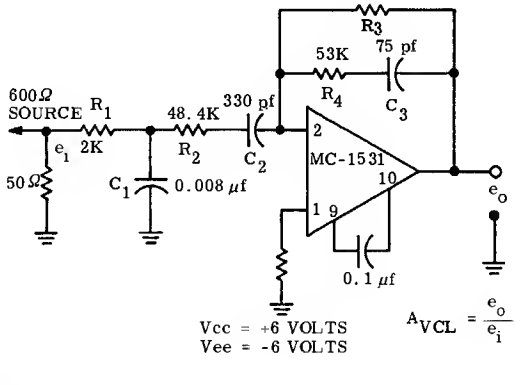


FIGURE 19

AN INTEGRATED CIRCUIT RF-IF AMPLIFIER

INTRODUCTION

A versatile integrated circuit for RF-IF applications is introduced which offers high gain, extremely low internal feedback, and wide AGC range. The circuit is a common-emitter, common-base pair (the cascode connection) with an AGC transistor and associated biasing circuitry. The amplifier is built on a very small die and is economically comparable to a single transistor, yet it offers performance advantages unobtainable with a single device. This application note describes the AC and DC operation of the circuit, a discussion of Y-parameters for calculating optimum power and voltage gain, and a variety of applications as an IF single-tuned amplifier, IF wideband amplifier, oscillator, video-audio amplifier and modulator. A discussion of noise figure is also included.

I. EXPLANATION OF OPERATION

The simplified schematic shown in Figure 1 will be used to quantitatively explain the A. C. and D. C. operation of the MC1550. Considering D. C. operation first, the voltage V_S and resistor R_S establish the current I_{D_1} in diode D_1. Since this diode is on the same silicon die as transistor Q_1 and they are laid out very close to each other, the emitter current of Q_1 will be within 5% of the diode current.* This biasing technique takes advantage of the matching characteristics that are available with integrated circuits and illustrates a method which would be difficult to accomplish with discrete components but with ease using I/C's. The current established in the emitter of Q_1 will be shared in some manner between Q_2 and Q_3 depending on the relationship between V_{AGC} and V_R in the same manner as a current mode switch or differential amplifier. For the case where V_{AGC} is at least 114 mV greater than V_R, Q_3 is turned off and all the collector current of Q_2 is transferred to Q_1. Since Q_3 is off, the A. C. gain will be at its minimum point. If, on the other hand, V_{AGC} is less than V_R by 114 mV or more, all the collector current present in Q_1 will flow through Q_3. This, then, is the operating point for maximum A. C. gain. Considering now the A. C. operation, the input is

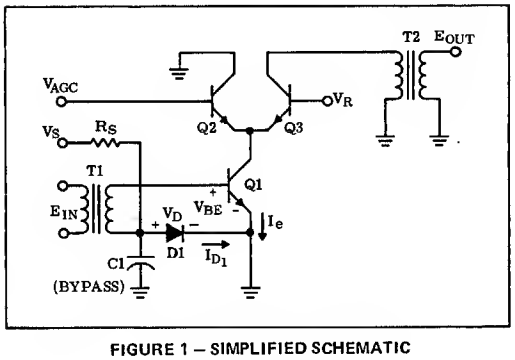


FIGURE 1 – SIMPLIFIED SCHEMATIC

applied to the base of Q_1 and the output taken from the collector of Q_3. Thus, the combination of Q_1 - Q_3 acts as a common-emitter common-base pair. This pair offers the distinct performance advantage of reducing internal feedback (Y_{12}) two orders of magnitude when compared to a single transistor. Using the General Radio 1607-A Immittance bridge, Y_{12} was unmeasurable up to frequencies of 300 MHz. This indicates that the magnitude of Y_{12} is less than 0.001 m-mhos over the useful frequencies of operation of the MC1550, and can, for all practical purposes, be neglected. The ability to vary the gain of this circuit can also be a performance advantage when compared to a single transistor. The following reasoning makes this apparent: As will be shown in the next section, changing the AGC voltage has a very minor effect on the operating point of Q_1; therefore, the input impedance of Q_1 remains constant. Thus, there is no detuning of the tuned input circuitry as performance curves of practical circuits shown in following sections will verify.

A schematic of the MC1550 amplifier including biasing resistors is shown in Figure 2. The circuit is constructed on a 30 x 32 mil die using 200 ohm/square sheet resistance material and 1 x 0.5 mil emitters in the box geometry transistors. Resistors R_1 and R_2 bias the diode D_1 and also establish a base voltage for transistor Q_3. Resistors R_3 and R_4 serve to widen the AGC voltage range from 114 mV to about 0.86 volts. This is necessary so that the AGC line will be less susceptible to external noise.

II. D. C. CALCULATIONS AND BIASING

A D. C. analysis which closely approximates the actual operation is as follows. Using Figure 3 and writing node equations for nodes 8 and 10, we have

for node 8,

$$\frac{V_8 - V_{CC}}{R_1} + \frac{V_8 - V_{10}}{R_3} + \frac{V_8 - V_{D_1}}{R_2} + I_{B_3} = 0$$

for node 10,

$$\frac{V_{10} - V_{AGC}}{R_4} + \frac{V_{10} - V_8}{R_3} + I_{B_2} = 0$$

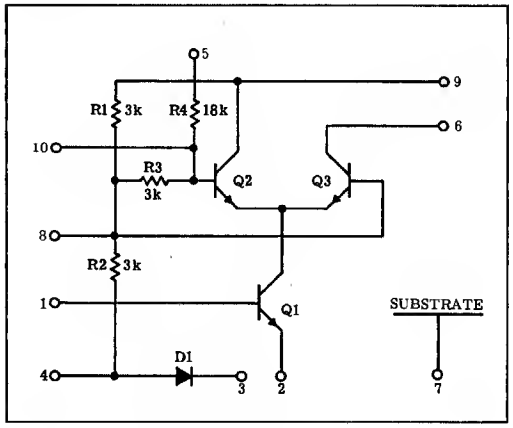


FIGURE 2 – MC1550 SCHEMATIC

*See Appendix A for derivation

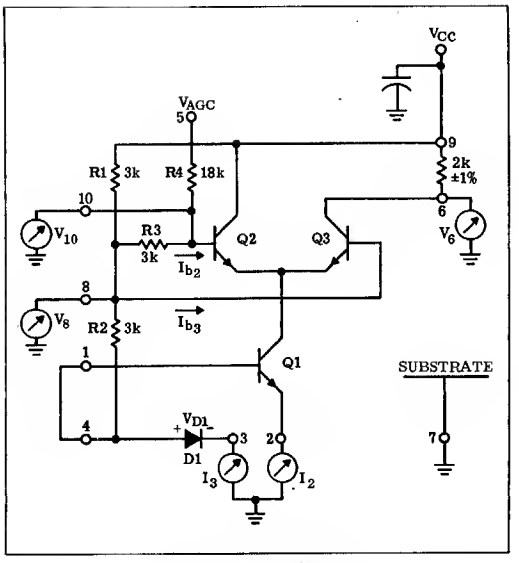


FIGURE 3 – DC BIASING

Neglecting I_{b_2} and I_{b_3} and solving for V_8 and V_{10}, we have

$$V_8 = \frac{\left[V_{CC} + \left(\frac{R_1}{R_2}\right)V_{D_1}\right]\left[1 + \frac{R_4}{R_3}\right] + V_{AGC}\left[\frac{R_1}{R_3}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]} \quad (1)$$

$$V_{10} = \frac{\left[V_{CC} + \left(\frac{R_1}{R_2}\right)V_{D_1}\right]\left[\frac{R_4}{R_3}\right] + V_{AGC}\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]} \quad (2)$$

From equations (1) and (2), observe that the D.C. voltages are dependent upon resistor ratios rather than absolute values. Present integrated circuit technology enables these tolerances to be held within 5% quite easily, thus achieving very good D.C. stability.

The manner in which transistors Q_2 and Q_3 share the current which passes through transistor Q_1 is determined by the difference of the base voltages, $V_8 - V_{10}$ (See Appendix B).

Define $V_0 = V_8 - V_{10}$, and subtracting (2) from (1):

$$V_0 = \frac{\left[V_{CC} + \left(\frac{R_1}{R_2}\right)V_{D_1}\right] - V_{AGC}\left[1 + \frac{R_1}{R_2}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]} \quad (3)$$

The change in equation (3) with AGC voltage may be calculated by differentiating,

$$\frac{\partial V_0}{\partial V_{AGC}} = \frac{-\left[1 + \frac{R_1}{R_2}\right]}{\left[1 + \frac{R_4}{R_3}\right]\left[1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right] - \left[\frac{R_1}{R_3}\right]\left[\frac{R_4}{R_3}\right]}$$

For the nominal case of $R_1 = R_2 = R_3 = R$ equation (3) simplifies to

$$\frac{\partial V_0}{\partial V_{AGC}} = \frac{-2}{3 + 2\left(\frac{R_4}{R}\right)} \quad (4)$$

which is, again, a function of a resistor ratio. Using nominal values of R = 3k ohms and R_4 = 18k ohms

$$\frac{\partial V_0}{\partial V_{AGC}} = -0.133\ \frac{\text{Volts}}{\text{Volt}} \quad (5)$$

Using (5), for a change in V_0 of 114 mV, the AGC voltage must change 0.86 volts at room temperature, which corresponds to measured values.

To determine the effect of the AGC voltage on the operating point of Q_1, the emitter current of Q_1 is calculated as a function of AGC voltage using Figure 4. Writing a node equation for the node at the base of Q_1:

$$\frac{V_8 - V_{D_1}}{R_2} = I_{D_1} + I_{B_1} \quad (6)$$

Assuming a close match of p-n junctions for diode D_1 and the base to emitter junction of Q_1,

$$I_{D_1} = I_{E_1} = (h_{FE} + 1)\, I_{B_1}$$

Substituting the above into (6):

$$V_8 - V_{D_1} = R_2\left(\frac{h_{FE} + 2}{h_{FE} + 1}\right) I_{E_1} \quad (7)$$

For $h_{FE} \gg 1$

$$I_{E_1} \approx \frac{V_8 - V_{D_1}}{R_2}$$

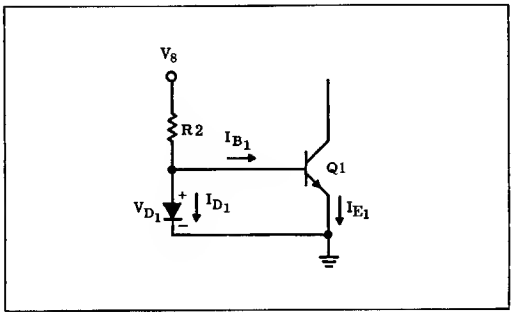


FIGURE 4 – BIASING OF INPUT TRANSISTOR

Substituting the value for V_8 from equation (1) into (7):

$$I_{E_1} = \frac{\left[V_{CC} + \left(\frac{R_1}{R_3}\right)V_{D_1}\right]\left[1 + \frac{R_4}{R_3}\right] + V_{AGC}\left[\frac{R_1}{R_3}\right]}{R_2\left[\left(1 + \frac{R_4}{R_3}\right)\left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right) - \left(\frac{R_1}{R_3}\right)\left(\frac{R_4}{R_3}\right)\right]} - \frac{V_{D_1}}{R_2} \quad (8)$$

To obtain the variation of I_{E_1} with V_{AGC}, (8) is differentiated:

$$\frac{\partial I_{E_1}}{\partial V_{AGC}} = \frac{\frac{R_1}{R_3}}{R_2\left[\left(1 + \frac{R_4}{R_3}\right)\left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_2}\right) - \left(\frac{R_1}{R_3}\right)\left(\frac{R_4}{R_3}\right)\right]} \quad (9)$$

For nominal values of $R_1 = R_2 = R_3 = 3k$, $R_4 = 18k$

$$\frac{\partial I_{E_1}}{\partial V_{AGC}} = 22\ \mu a/volt \quad (10)$$

For a supply voltage $V_{CC} = 6.0V$, $I_{E_1} \approx 0.88$ mA, thus for full AGC operation (0.86V), the change in I_{E_1} is $19\mu A$ or 2.16%. For larger supply voltages, the effect of AGC voltage on I_{E_1} is even less (1% for $V_{CC} = 12.0V$). Since I_{E_1} varies only slightly, the input impedance variation (which depends on $r_e = KT/qI_E$) is very small. This fact is shown by the measured 60 MHz data in Figure 5.

III. TEMPERATURE STABILITY

The ability of the diode current to closely track the emitter current in Q_1 will give a good indication of the circuit's gain stability with temperature. A curve of I_{D_1}/I_{E_1} vs temperature is shown in Figure 6. The absolute variation of I_{E_1} is also shown on the curve for $V_{CC} = 6.0V$. The variation of I_{E_1} produces a measured variation in power gain of ±1.5 dB over the temperature range -55°C to +125°C, which will be explained in more detail in following sections.

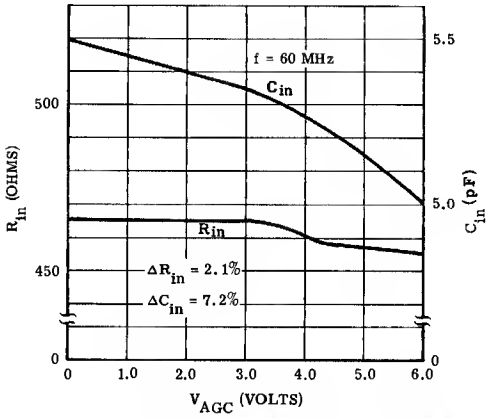


FIGURE 5 – INPUT RESISTANCE AND CAPACITANCE versus AGC VOLTAGE

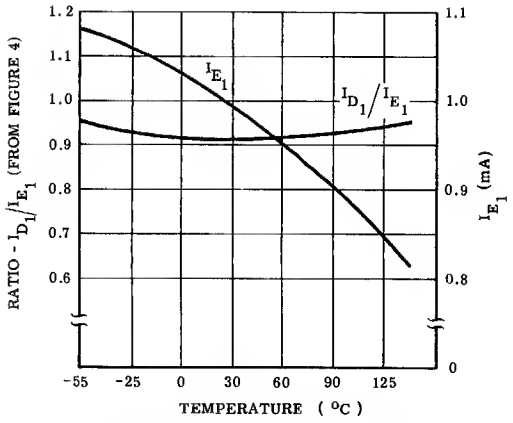


FIGURE 6 – DC CURRENTS versus TEMPERATURE

IV. CIRCUIT CHARACTERIZATION AND Y-PARAMETERS

There are two basic methods by which integrated circuits may be characterized. The first method is based on measurement or calculation of internal transistor parameters, forming of a suitable model for each, combining with other internal components and transistor models to form a overall model which will approximate the actual circuit. For integrated circuits which contain more than one or two active devices combined with distributed substrate capacitance and resistor parasitic capacitance, this method of analysis becomes difficult and the accuracy of results depends upon the accuracy of the model. This type of formulation has value in helping to relate specific circuit applications to device parameters. However, the accuracy of predicted performance is not quite as good as that obtainable when measured two-port parameters are used. The two-port method characterizes the linear active network as a black box, and is not limited by approximations but by the accuracy of measurement of the parameters. This method has the additional advantage of being amenable to well established design techniques. The MC1550 is characterized on the data sheet in terms of y-parameters which were measured on both the Boonton R-X meter and the General Radio 1607A Immittance bridge. The correlation between the two instruments was ±5% where frequencies overlapped. Therefore, the y-parameters will be used in later sections for circuit design, and predicted and measured performance are very close to each other. However, in order to better understand the reasons for some of the values of y-parameters obtained, a y-parameter discussion is in order.

To discuss the y-parameters of the MC1550, it is convenient to consider the circuit as a common-emitter, common-base cascode as shown in Figure 7. The circuit has been analyzed in reference 3, but the method is repeated here for clarity. To derive the y-parameters, the transmission matrix for a common-emitter and common-base stage may be used as in Figure 7. The overall transmission matrix then becomes:

$$\begin{bmatrix} e_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A_1 A_2 + B_1 C_2 & A_1 B_2 + B_1 D_2 \\ A_2 C_1 + C_2 D_1 & B_2 C_1 + D_1 D_2 \end{bmatrix} \begin{bmatrix} e_2 \\ i_2 \end{bmatrix} \quad (11a)$$

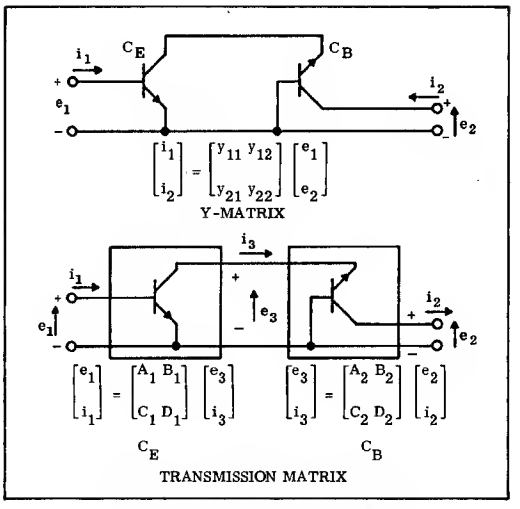


FIGURE 7 – CE-CB MATRIX PARAMETERS

The y-parameters of each stage in the cascode circuit are related to the above transmission factors as follows:

$$A_1 = -\frac{y_{oe}}{y_{fe}} \quad B_1 = -\frac{1}{y_{fe}} \quad A_2 = -\frac{y_{ob}}{y_{fb}} \quad B_2 = -\frac{1}{y_{fb}}$$

$$C_1 = -\frac{\Delta y}{y_{fe}} \quad D_1 = -\frac{y_{ie}}{y_{fe}} \quad C_2 = -\frac{\Delta y}{y_{fb}} \quad D_2 = -\frac{y_{ib}}{y_{ob}}$$

where $\Delta y = y_i y_o - y_f y_r$

and $y_{fe} = y_{21}$ common-emitter

$y_{fb} = y_{21}$ common-base, etc.

At this point, the y-parameters may be substituted for the transmission parameters in the overall matrix and then a conversion may be made from an overall transmission matrix to an overall y-parameter matrix by using the equations below:

$$Y_{11} = \frac{D}{B} \quad Y_{12} = -\frac{\Delta T}{B}$$

$$Y_{21} = -\frac{1}{B} \quad Y_{22} = \frac{A}{B}$$

where $\Delta T = AD - BC$

and $A = A_1A_2 + B_1C_2 \quad B = A_1B_2 + B_1D_2$

$C = A_2C_1 + C_2D_1 \quad D = B_2C_1 + D_1D_2$.

The above set of equations may be manipulated into several forms. However, with the use of the relationship between the common-emitter and common-base y-parameters, the overall y-parameters may be put into the useful form presented in reference 3.

$$Y_{ib} = y_{ie} + y_{re} + y_{fe} + y_{oe}$$

$$Y_{rb} = -(y_{re} + y_{oe})$$

$$Y_{fb} = -(y_{fe} + y_{oe})$$

$$Y_{ob} = y_{oe} \tag{11b}$$

The results of these manipulations are listed in equations 12 through 15 below.

$$Y_{11} = \frac{y_{ie}(y_{oe} + y_{ib}) - y_{fe}y_{re}}{(y_{oe} + y_{ib})} \approx y_{ie} \tag{12}$$

$$Y_{12} = -\frac{y_{re}y_{rb}}{y_{oe} + y_{ib}} \tag{13}$$

$$Y_{21} = -\frac{y_{fe}y_{fb}}{(y_{oe} + y_{ib})} \approx -y_{fe} \tag{14}$$

$$Y_{22} = \frac{y_{ob}(y_{oe} + y_{ib}) - y_{rb}y_{fb}}{(y_{oe} + y_{ib})} \approx y_{ob} \tag{15}$$

Where Y_{11}, Y_{12}, etc. denote the y-parameters of the cascode circuit. At this point, either calculations or measurements on common-emitter and common-base parameters for the individual transistors may be used to verify and explain the overall y-parameters. For the MC1550, individual transistors were bonded into a TO-18 package for these purposes. The results of both measurements and calculations indicate that the conculsions below are correct:

1. The input admittance of the cascode circuit is within 5% of the input admittance of a common-emitter transistor.
2. The reverse transfer admittance is extremely low since, in terms of milli-mhos, it involves the product of two numbers less than unity, divided by a number greater than one. Hence, the fact that it is extremely difficult to measure is understandable.
3. The forward transfer admittance is primarily that of a common-emitter transistor.
4. The output admittance is essentially that of a common-base amplifier (very low real part and an imaginary part controlled by the parasitic capacitance of a monolithic transistor).

These conclusions will be used to some extent in each of the applications in later sections of this note. Typical measured values of y-parameters versus frequency and versus AGC voltage are shown in Figures 8 through 11, and will be used in the following sections for designing tuned amplifiers. The y_{12} parameter is not shown since it was found to be less than 0.001 m-mhos, therefore, it will be neglected in examples to follow.

V. NOISE CONSIDERATIONS

The noise performance of all possible cascoded integrated circuit pairs has been theoretically evaluated in reference 2. Two major points that are results of this analysis should be repeated here:

1. The noise figure of a small geometry monolithic transistor is very closely the same as that of a discrete bottom collector transistor which has the same geometry.

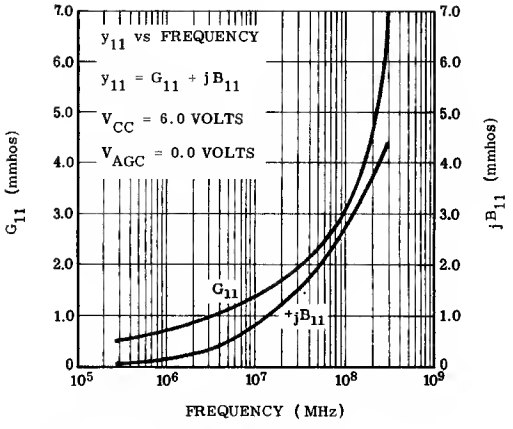


FIGURE 8 – INPUT ADMITTANCE versus FREQUENCY

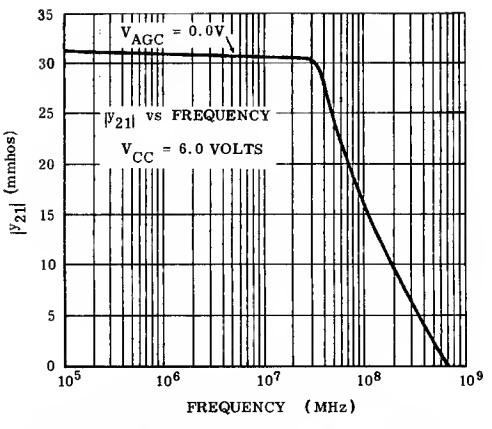


FIGURE 11 – MAGNITUDE OF FORWARD TRANSFER ADMITTANCE versus FREQUENCY

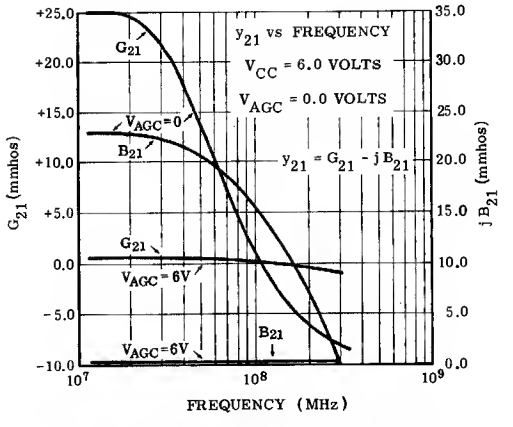


FIGURE 9 – FORWARD TRANSFER ADMITTANCE versus FREQUENCY

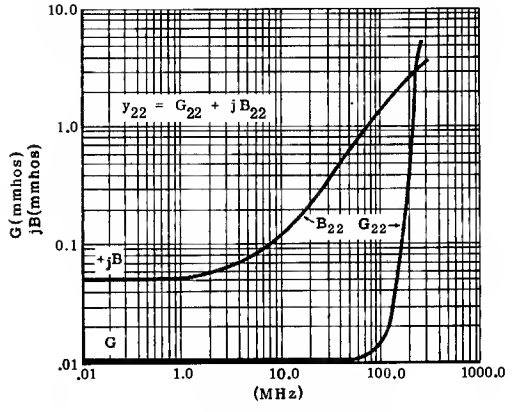


FIGURE 10 – OUTPUT ADMITTANCE versus FREQUENCY

2. Of all possible connections of two transistors, the best noise figure will be obtaineo when the input device is in the common-emitter connection. The second device will have little or no influence on noise figure.

The MC1550 amplifier, therefore, should follow closely that of it's discrete counterpart in the common-emitter connection. That this is true is seen in Figure 12 which shows a curve of optimum noise figure and optimum source resistance versus frequency.

VI. APPLICATIONS

NARROW BAND TUNED AMPLIFIER (CE-CB)

This section considers the design of a single stage, 60 MHz amplifier. A typical circuit for this application is shown in Figure 13. The following two-port y-parameters are obtained from the curves in figures 8 through 11 at 60 MHz, for V_{CC} = 6.0, and V_{AGC} = 0.0

$$y_{11} = 2.50 + j2.3 = 3.34 \angle 42.6^{o} \text{ mmhos}$$

$$y_{12} = \text{(negligible)}$$

$$y_{21} = 10.0 - j19.0 = 21.5 \angle -62.3^{o} \text{ mmhos}$$

$$y_{22} = 0.01 + j0.80 = 0.80 \angle 90^{o} \text{ mmhos}$$

Since y_{12} has been neglected, the maximum available gain (MAG) is assumed to exist and may be calculated from the equation (16) below:

$$MAG = \frac{\text{Power Available at Output}}{\text{Power Available from Source}} = \frac{|y_{21}|^2}{4\, R_e(y_{11})\, R_e(y_{22})} \qquad (16)$$

MAG = 4620 and 10 log (MAG) = 36.7 dB

This is the theoretical maximum limit for this circuit at this frequency. Another important measure of power gain is transducer gain, G_T, defined by the equation

$$G_T = \frac{\text{Power Delivered to the Load}}{\text{Power Available from the Source}} = \frac{P_o}{P_{AVS}} \qquad (17)$$

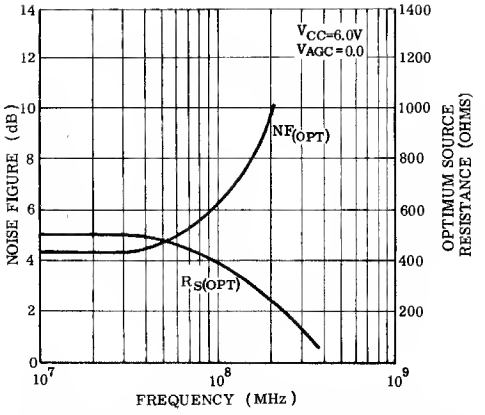


FIGURE 12 – NOISE FIGURE versus FREQUENCY OPTIMUM SOURCE RESISTANCE versus FREQUENCY

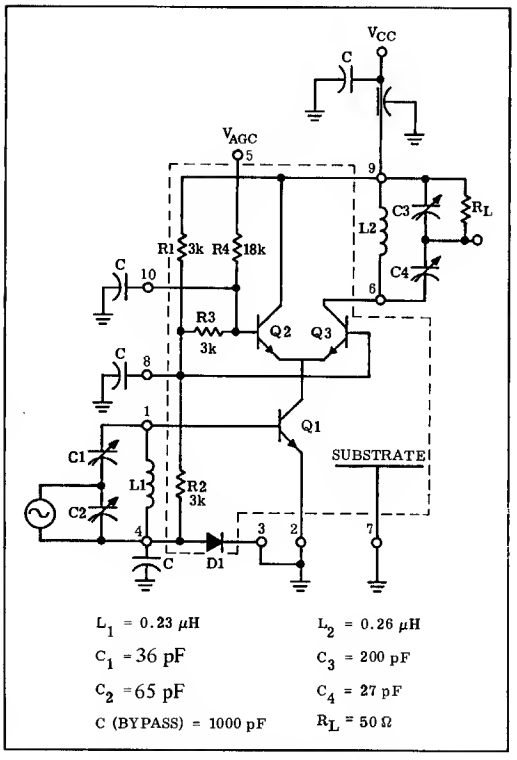


FIGURE 13 – 60 MHz TUNED AMPLIFIER

It can be shown* that maximum power gain through a linear two-port network occurs when the source admittance is the complex conjugate of the input admittance of the network and the load admittance is the complex conjugate of the output admittance of the network. From basic two-port analysis using y-parameters, the formulas for input and output admittances are:

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L} \tag{18}$$

$$Y_{out} = y_{22} - \frac{y_{12}y_{21}}{y_{11} + Y_S} \tag{19}$$

Since the assumption has been made that y_{12} is zero,

$$Y_{in} \approx y_{11}$$

$$Y_{out} \approx y_{22}$$

Therefore, the optimum source and load admittances are given by:

$$y_{S(opt)} = y_{11}^* = 2.50 - j2.30 \text{ mmhos}$$

$$y_{L(opt)} = y_{22}^* = 0.01 - j0.80 \text{ mmhos}$$

These values of Y_S and Y_L are not exact, but they do turn out to be very close to the final values obtained in the laboratory. Having calculated $y_{S(opt)}$ and $y_{L(opt)}$, G_T may be calculated:

$$G_T = \frac{4|y_{21}|^2 R_c(y_S) R_c(y_2)}{|(y_{11} + y_S)(y_{22} + y_L) - y_{12}y_{21}|^2} \tag{20}$$

Using values found above: $G_T = 4620$ or $G_T = 36.7$ dB.

The value for G_T is equal to the available power gain which also follows since $y_{12} \approx$ zero. In practice, it is difficult to achieve the calculated theoretical value of transducer power gain because of the losses in the inductors. The finite value of unloaded Q for a practical inductor results in an equivalent resistance which will load the output and restrict both the bandwidth and the power gain. As will be seen in the following section, the equivalent R_P can be used to modify y_{22} and then the calculation performed with the new y_{22}'.

Due to the low value of y_{12}, the assumption that the output load can be varied without affecting the input is valid and can be used to advantage in this design. Consider first the input tuned network and the input admittance as shown in the circuit of Figure 14(a). There are many ways to proceed with the design, and the method chosen here is to arbitrarily broad-band the input network and design the matching network to conjugate match y_{11}. The matching network[1] then transforms the 50 ohm source into y_{11}^*. Using techniques in reference 1 the calculated values of L_1, C_1, and C_2 are:

$$L_1 = 0.23 \ \mu H$$

$$C_1 = 36 \text{ pF}$$

$$C_2 = 65 \text{ pF}$$

*See Reference 1

[1]Chapter 13 of reference 1 details a design procedures for matching networks.

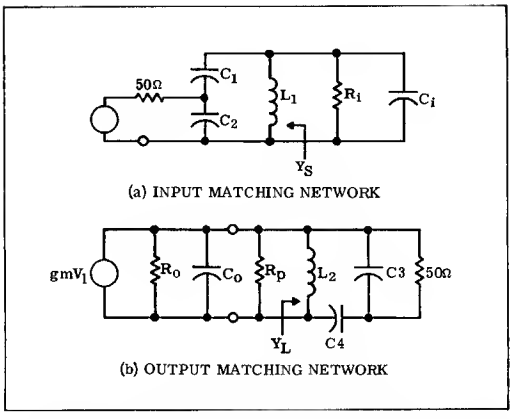


FIGURE 14 – INPUT AND OUTPUT MATCHING NETWORKS

Considering now the output matching network in Figure 14(b), the bandwidth should be considered first:

$$BW = \frac{1}{2\pi R_T C_T}$$

R_T = Total R at the output

C_T = Total C at the output

In Figure 14(b), resistor R_P is the equivalent resistance across the output caused by the finite unloaded Q of L_2. The measured value of R_P is 35k ohms at 60 MHz. This value may be placed in parallel with the value of R_O, and the resultant R used to calculate a new $y_{22} = y'_{22}$. The new value of y_{22} will be used to design the matching network so that the load admittance is the complex conjugate of y'_{22}. The total R and total C across the output may then be traded to achieve the required bandwidth and transducer power gain and L may be varied to maintain the desired center frequency. For R_P = 35k ohms, the new y_{22} is:

$$y'_{22} = 0.039 + j0.80 \quad \text{mmhos}$$

then

$$y_L = 0.039 - j0.80 \quad \text{mmhos}$$

The matching network values are then calculated:

$$L_2 = 0.26\ \mu H$$

$$C_3 = 630\ pF$$

$$C_4 = 27\ pF$$

The total R and C present across the output is:

$$\frac{1}{R_T} = 2\,(0.039)\,10^{-3} \qquad C_T = C_0 + C_{\text{(Matching network)}}$$

R_T = 12.5k ohms $\qquad C_T$ = 28 pF

These values may then be used with y-parameters to calculate the transducer power gain, center frequency, and bandwidth. The results are:

f_o = 60 MHz

G_T = 30.1 dB

BW = 0.5 MHz

Using the values of L and C previously calculated, the circuit of Figure 13 was constructed and tested in the laboratory. The results using 4 different MC1550's are:

Circuit No.	Center Frequency	Transducer Power Gain	Bandwidth
1	60 MHz	30.0 dB	0.6 MHz
2	60 MHz	30.0 dB	0.5 MHz
3	60 MHz	30.5 dB	0.6 MHz
4	60 MHz	30.4 dB	0.4 MHz

No retuning was done when the units were interchanged, which accounts for the slight differences in measured values. The AGC characteristics of the amplifier are shown in Figure 15. The center frequency and bandwidth are very constant over a 40 dB AGC range and the bandwidth varies ± 0.15MC for a 55 dB AGC range. This stability is due mostly to the fact that input impedance does not change with AGC, and because the input tuned circuitry is broad-banded. The design in the next section will show only small variations in center frequency and bandwidth (less than 3%) when the input tuning network is a narrow-band circuit.

The performance of the circuit over the temperature range -55°C to +125°C is shown in Figure 16. The worst variation was -2 dB over the complete range.

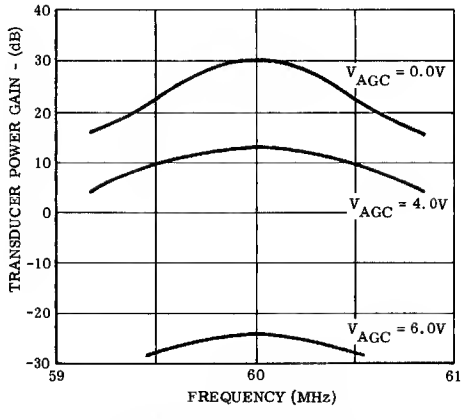


FIGURE 15 – 60 MHz SINGLE STAGE AMPLIFIER GAIN

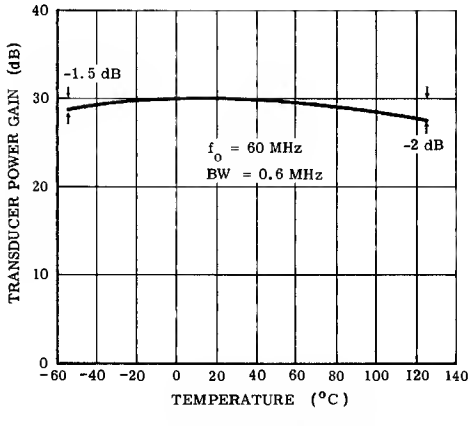


FIGURE 16 – 60 MHz POWER GAIN versus TEMPERATURE

WIDEBAND TUNED AMPLIFIER

The foregoing example demonstrates the high gain of the MC1550 at the expense of bandwidth. This narrow bandwidth is primarily due to the large value of resistance which is across the parallel tuned output circuit. Reducing this value of resistance will broaden the bandwidth and reduce the power gain so that more than one stage may be required to achieve the specified gain and bandwidth. This section is concerned with the design of a multi-stage amplifier to illustrate the above points. The amplifier specifications are:

Single Tuned
Center Frequency – 45 MHz
Bandwidth – 15 MHz
Transducer Power Gain – 30 dB

For this application, it will be necessary to use a two-stage amplifier. Because there will be three tuned circuits, there will be a bandwidth reduction according to the following equation:

$$BW_{OVERALL} = BW_{STAGE}\sqrt{2^{1/n} - 1}$$

where n is the number of tuned circuits.

Thus, for an overall bandwidth of 15 MHz, each stage should be designed for 30 MHz bandwidth. From the curves given in Figures 8 through 10, the y-parameters at 45 MHz, V_{cc} = 6.0V, V_{AGC} = 0.0V are as follows:

y_{11} = 2.5 + j2.0 mmhos

y_{12} = (negligible)

y_{21} = 16 - j21 mmhos

y_{22} = 0.01 + j0.55 mmhos

For the following calculations, the source and load impedance are 50 ohms.

The simplified circuit shown in Figure 17 will be used for this design. For this circuit, a new output resistance for each network can be found in order to simplify the calculations. By doing this, the two-port is extended as shown by the dashed lines in Figure 17. This value of R is the parallel combination of R_o and R_L. From the value of y_{22}, R_o is found to be 100k. Assuming that y_S can be accurately transformed into y_{11}^* and $y_L = y_{22}^*$, the value of R_L which will give the required gain of 15 dB for each stage can be found from the transducer power gain as shown in equation 21:

$$G_T = \frac{|y_{21}|^2}{4\,R_e(y'_{22})\,R_e(y_{11})} \quad . \qquad (21)$$

For the values given, $R_e(y'_{22})$ = 2.88 mmhos

Then,

$$\frac{R_o R_L}{R_o + R_L} = \frac{1}{R_e(y'_{22})}$$

Solving, $R_{L(min)}$ = 350 ohms

Let R_L = 500 ohms to realize the specified transducer power gain.

Inductors with an unloaded Q of 30 or more must be used so that the effect of their resistance on R_L can be neglected. Using the equations for center frequency and bandwidth of a tuned circuit,

$$F_o = \frac{1}{2\pi\sqrt{LC}} \qquad BW = \frac{1}{2\pi RC}$$

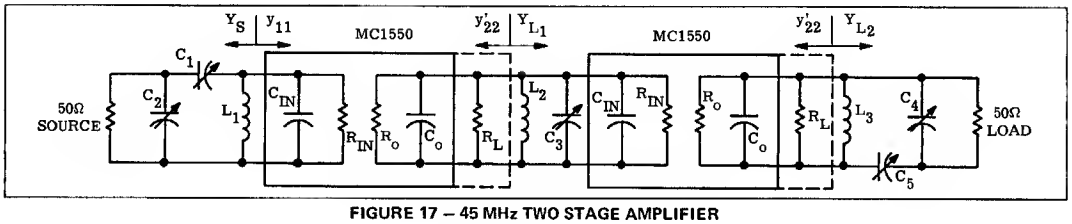


FIGURE 17 – 45 MHz TWO STAGE AMPLIFIER

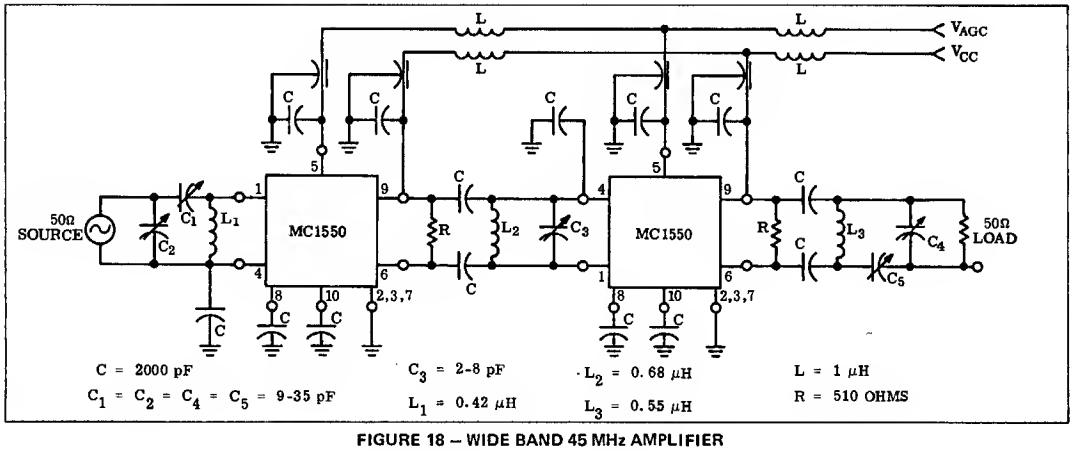


FIGURE 18 – WIDE BAND 45 MHz AMPLIFIER

the necessary value of L and C at each interstage may be found. These values are:

C_1 = 25 pF (9-35) L_1 = 0.42 μH R_L = 510Ω

C_2 = 20 pF (9-35) L_2 = 0.68 μH

C_3 = 5 pF (2-8) L_3 = 0.55 μH

C_4 = 20 pF (9-35)

C_5 = 25 pF (9-35)

The circuit of Figure 18 was built and the table below indicates the measured values of transducer power gain and bandwidth.

Unit	Center Frequency	Gain (dB)	Bandwidth
1	45 MHz	30.2	15.4 MHz
2	45 MHz	30.5	15.0 MHz
3	45 MHz	31.0	14.5 MHz
4	45 MHz	30.3	14.2 MHz

The practical circuits closely follow the predicted values previously calculated. The AGC characteristic is shown in Figure 19; and, as before, the bandpass characteristics are preserved over the entire AGC range.

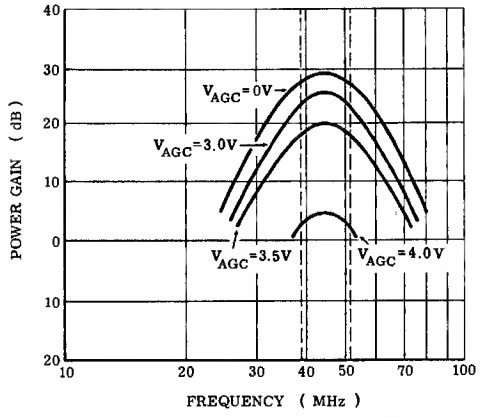


FIGURE 19 – AGC CHARACTERISTICS OF 45 MHz WIDE BAND AMPLIFIER

A STAGGER TUNED I-F STRIP

The term "stagger tuning" refers to an amplifier comprising several stages in cascade, in which the stages are not tuned to the same frequency but are "staggered" at frequencies above and below the desired center frequency. Not only are the tunings of the individual stages not identical, but often their bandwidths are also different. Although the advantages of this method were apparent to a few persons several years earlier, the credit for first exploiting the stagger tuning technique in detail belongs to Henry Wallman. [5] Since that time, many authors have extended Wallman's work and the technique is well documented.

The objectives of stagger tuning are twofold: (1) A gain-bandwidth product is achieved which is greater than that of synchronously tuned cascade stages, and (2) it is possible to achieve a selectivity curve of prescribed amplitude response. Thus it is possible to stagger tune n single stages as to achieve a flat bandpass, an equal ripple (Chebyshev) bandpass, or numerous other selectivity curves with very good gain. A design procedure for a maximally flat stagger tuned amplifier and laboratory results are given in the following section.

DESIGN PROCEDURE

Consider the following hypothetical design for an IF amplifier:

Center Frequency (fo)	45 MHz	Stagger Tuned	
Bandwidth (Δf)	6 MHz	Source Impedance	50Ω
Power Gain (G_T)	70 dB	Load Impedance	50Ω
AGC Control	>50 dB		

A typical circuit for this application using transformer interstage coupling is shown in Figure 20. The individual stage requirements of this flat staggered amplifier are as follows:

a. One stage tuned to f_0 with bandwidth Δf.
b. One stage tuned to $f_0 \alpha$ with $Q = 2.0/\delta$
c. One stage tuned to f_0/α with $Q = 2.0/\delta$

where $\delta = \Delta f/f_0$ and $\alpha = 1 + 0.433\delta$

For the amplifier specifications given above, the following results are obtained:

$\delta = 0.1333$ $\alpha = 1.0578$

a. One stage tuned to 45 MHz with a 6 MHz bandwidth.
b. One stage tuned to 47.60 MHz with a 3 MHz bandwidth.
c. One stage tuned to 42.50 MHz with a 3 MHz bandwidth.

There is nothing new or tricky involved in the interstage design. The most expedient procedure is to assume that the coupling transformers are ideal, form equivalent models with one side of the transformer referred to the other side, then compute the bandwidth and center frequency from the equations for the parallel tuned circuits:

$$\Delta f = \frac{1}{2\pi R_T C_T} \qquad f = \frac{1}{2\pi\sqrt{L_T C_T}}$$

where R_T = total parallel resistance
C_T = total parallel capacitance
L_T = total parallel inductance

However, due to the fact that there are two tuned circuits associated with each stage, there will be an overall bandwidth shrinkage of each stage. This is easily handled by broadbanding the output tuned circuit of Stage 1 while achieving the desired selectivity and bandwidth with the

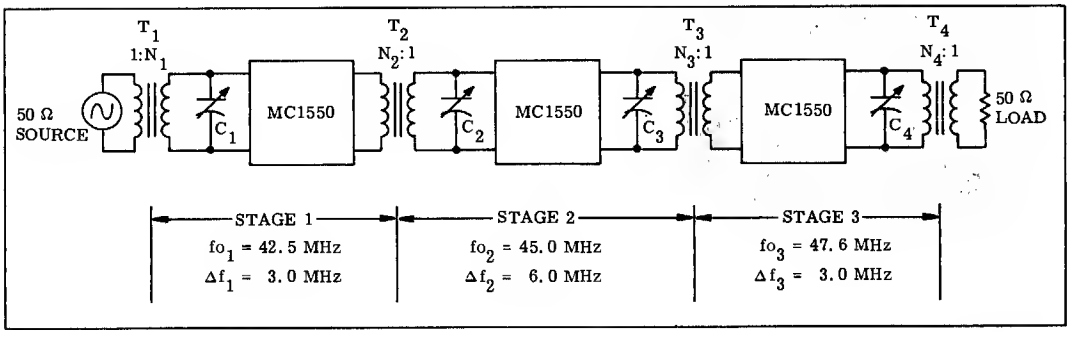


FIGURE 20

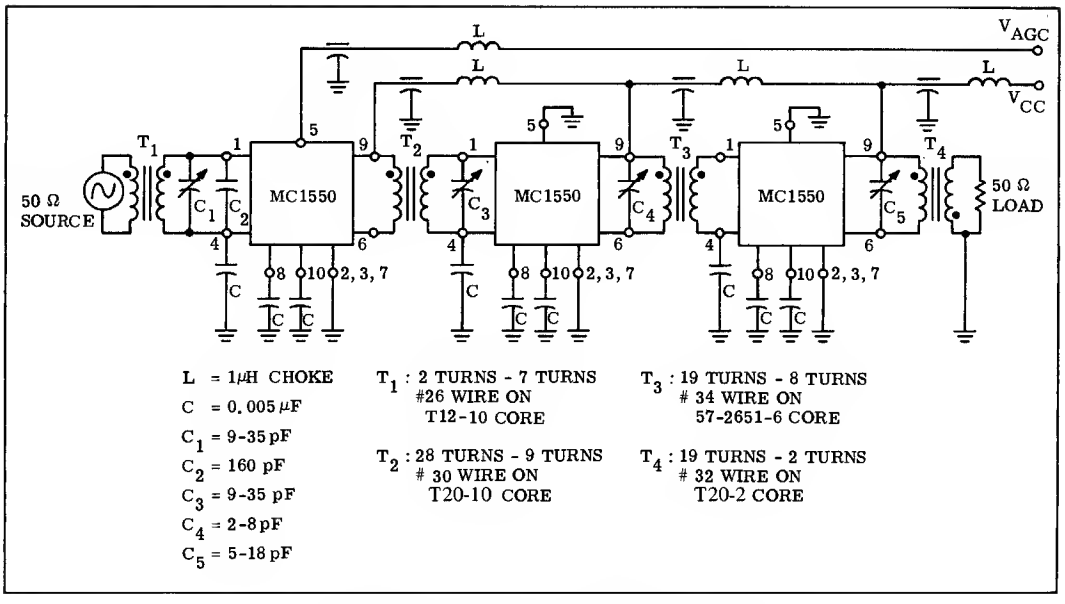


FIGURE 21 – 45 MHz STAGGER TUNED AMPLIFIER

input tuned circuit and visa versa with Stage 3. The same procedure could be followed in the design of Stage 2 by broadbanding the output tuned circuit while achieving the desired bandwidth and selectivity with the input tuned circuit. However, for this particular circuit, the procedure taken was to synchronously tune both the input and output circuits of Stage 2 and take into account the shrinkage factor. A schematic of the final design showing all pin connections is given in Figure 21.

TUNING

As was pointed out earlier, one very important characteristic of the MC1550 is the ease with which it is tuned. The first prototype circuit was tuned as follows: each stage was disconnected from the other stages and loading applied to each stage to simulate the actual circuitry in cascade. Each stage was then tuned to the desired center frequency with the correct bandwidth. Once each stage was tuned, the circuits were connected in cascade and final fine tuning adjustments made. With the experience gained in tuning the first prototype, the second prototype was tuned by merely sweeping the amplifier with a Jerrold 890 sweep generator and tuning while observing the output on an oscilloscope. A photograph of the sweep is shown in Figure 22. The final results were: Center frequency - 45 MHz, Bandwidth - 6 MHz, and Power Gain - 70.0 dB.

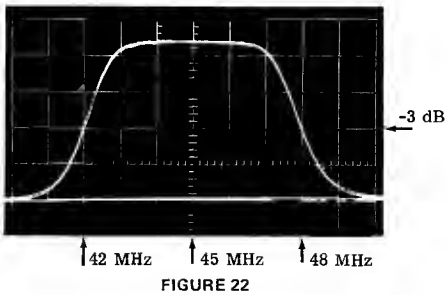


FIGURE 22

AGC CHARACTERISTICS

The choice of which stage or stages are to be AGC'd is more or less arbitrary. Various AGC combinations of the three stages were tried to study their effectiveness. With the AGC applied only to the first stage, 64 dB of AGC control was obtained with a maximum deviation from flatness in the passband of 0.7 dB. With the AGC applied to all three stages, 90 dB of AGC control was obtained, with a maximum deviation from flatness in the passband of 1 dB. These two conditions represent the minimum and maximum extremes. When the combinations of the three stages taken two at a time were tried, they all fell within the above range. Thus for the design specification, it was sufficient to AGC only the first stage. The variation of bandwidth and center frequency were measured and the results are shown in Figure 23. This data indicates a maximum of 5% bandwidth deviation occurring at the low gain (maximum AGC) condition, with full AGC occurring over a 2.5 volt range. With an input of 50μ volts rms, the output signal into 50 ohms is 156 mvolts with a noise level of 6.8 mvolts.

The results of this design strongly indicate that the MC1550 has tremendous potential for use in both the R-F and I-F stages of television, radio, radar, and communication gear where high gain, wide AGC control, and low cost are of prime importance.

AGC Voltage	Power Gain dB	Center Frequency MHz	Bandwidth MHz
0.0	70.0	45.0	6.0
0.5	70.0	45.0	6.0
1.0	70.0	45.0	6.0
1.5	70.2	45.0	6.0
2.0	70.2	45.0	6.0
2.5	63.5	45.0	5.9
3.0	58.4	45.0	5.8
3.5	46.1	45.0	5.8
4.0	28.7	45.0	5.8
4.5	6.2	45.0	5.7

FIGURE 23

OSCILLATOR

The MC1550 can conveniently be used as an oscillator in both the CE-CB and CC-CB configurations. In this section, the CE-CB configuration will be analyzed to determine the factors that will influence the frequency of oscillation, and a practical circuit given for a 5-10 MHz oscillator. Consider first the fundamentals of oscillator operation from Figure 24. The closed loop voltage gain of Figure 24 is given by:

$$A_{CL} = \frac{e_0}{e_1} = \frac{A_{OL}(\omega)}{1 - A_{OL}(\omega)\,\beta(\omega)} \qquad (22)$$

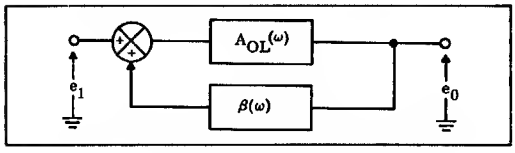


FIGURE 24 – BASIC FEEDBACK AMPLIFIER

Where A_{OL} represents the open-loop gain of the amplifier with the output of the amplifier loaded by the input impedance of the feedback network, $\beta(\omega)$. From equation 22, the closed-loop gain increases without bound when

$$A_{OL}(\omega)\,\beta(\omega) = 1 \qquad (23)$$

and self-sustained oscillations result. This equation indicates that the frequency of oscillation can be found by setting the imaginary component of $A_{OL}\,\beta(\omega)$ equal to zero. Once the frequency of oscillation, ω_0, has been determined, $\beta(\omega_0)$ can be found, and the threshold gain, A_T, below which oscillations will not be sustained may be determined from equation 24 below:

$$A_T(\omega_0) = \frac{1}{\beta(\omega_0)} \qquad (24)$$

This is the approach which will be used in analyzing the MC1550. With a signal applied to the base of transistor Q_1, the MC1550 acts as a common-emitter, common-base amplifier with high voltage gain and 180° phase shift at low frequencies. Because of the internal 180° phase shift, the $\beta(\omega)$ network must introduce an additional 180° phase shift from the output terminal (pin 6) to the input terminal (pin 1) so that positive feedback will result.

Although this phase shift can be accomplished by a number of methods, perhaps the easiest method of achieving it is the use of an inverting transformer connection. This method is shown in Figure 25. A simplified analysis of this circuit is as follows: Assuming first an ideal transformer, the voltage appearing at the input terminal is:

$$e_1 = -\frac{1}{n}\,e_0 \qquad (25)$$

By definition,

$$\beta(\omega) = \frac{e_1}{e_0}$$

so that

$$\beta(\omega) = -\frac{1}{n} \qquad (26)$$

Substituting equation 26 into equation 2:

$$A_{OL}\left(-\frac{1}{n}\right) = 1$$

or

$$A_{OL} = -n \qquad (27)$$

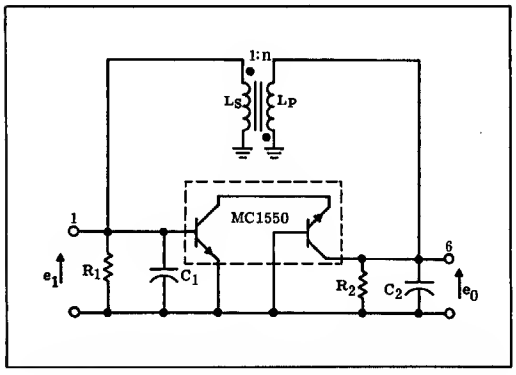


FIGURE 25 – TRANSFORMER COUPLED FEEDBACK AMPLIFIER

Hence, the open-loop gain must be equal to or greater than the turns ratio of the ideal transformer. From the discussion given in the video amplifier section of this application note, the expression for the low frequency voltage gain is:

$$A_V = -\frac{R_L}{r_{e_1}} \qquad (28)$$

Where R_L is the output load of the device and r_{e_1} is the dynamic emitter resistance of transistor Q_1 and is given by

$$r_{e_1} = \frac{26\ (mV)}{I_e\ (mA)}\ \text{(at room temperature.)}$$

From Figure 26, the equivalent load on the amplifier is:

$$R_L = R_o \parallel R_2 \parallel r_p \parallel n^2 R_1 \qquad (29)$$

where

R_o = the output resistance of the MC1550

R_2 = external load resistor

r_p = resistance of the transformer coil

$r_p = (Q_{\text{unloaded of coil}}) \cdot (\omega L_p)$

$n^2 R_1$ = resistance reflected into the primary from the secondary due to the transformer action

$\parallel$ denotes the parallel combination.

The expression of the open-loop gain now becomes

$$|A_{OL}| = \frac{R_o \parallel r_p \parallel R_2 \parallel n^2 R_1}{r_{e_1}} \qquad (30)$$

Substituting equation 30 into equation 27, the condition for self-starting and sustained oscillation is

$$\frac{R_o \parallel r_p \parallel R_2 \parallel n^2 R_1}{n r_{e_1}} \geq 1\ . \qquad (31)$$

The frequency of oscillation of the circuit is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_p\left(C_2 + \frac{C_1}{n^2}\right)}} \qquad (32)$$

Although the above equations were derived for an ideal transformer, the same method of analysis will be valid for the non-ideal transformer case. Using the model given in Figure 26, the same procedure used above may be repeated to solve for the minimum value of gain and the frequency of oscillation. This analysis is detailed in Appendix C, and the results are:

$$f_{osc} = \frac{1}{2\pi\sqrt{(1-K^2)\,L_P C_T}} \quad \text{For } K<1 \qquad (33)$$

$$A_T(\omega_0) = -\alpha \quad \text{Where } \alpha = K\sqrt{\frac{L_P}{L_S}} \qquad (34)$$

(See Appendix C for definition of terms).

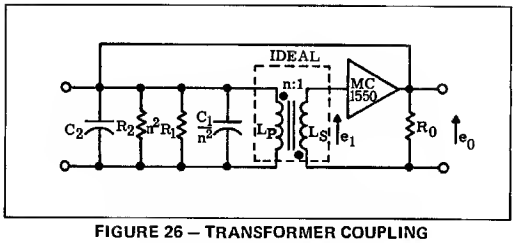


FIGURE 26 – TRANSFORMER COUPLING REFERRED TO PRIMARY

The circuit shown in Figure 27 was designed using the above equations, to obtain an output frequency that is variable from 5 to 10 MHz. The curve in Figure 28 shows the relationship between the value of C_2 and the frequency of oscillation for both measured and calculated values using equations 32 and 33.

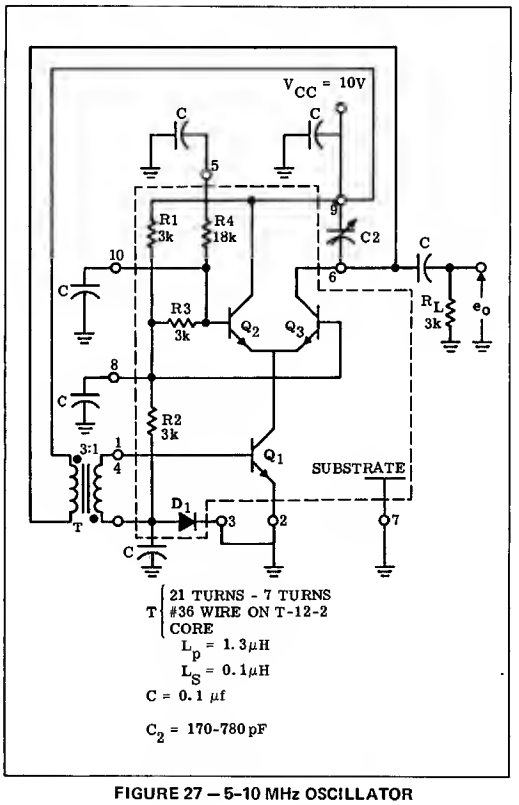


FIGURE 27 – 5-10 MHz OSCILLATOR

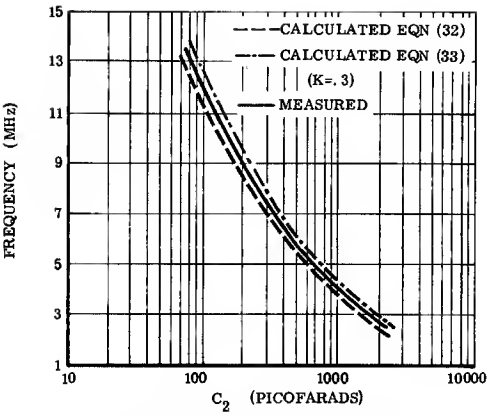


FIGURE 28 – FREQUENCY versus C_2

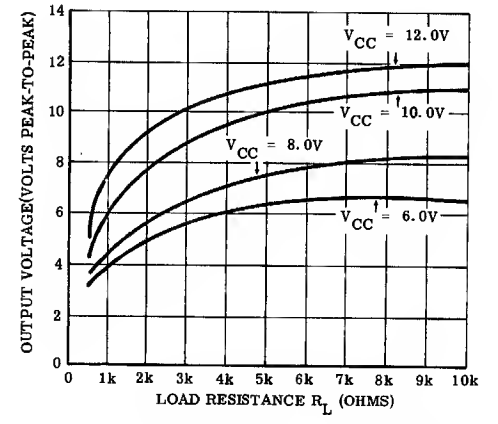


FIGURE 29 – OUTPUT VOLTAGE versus LOAD RESISTANCE

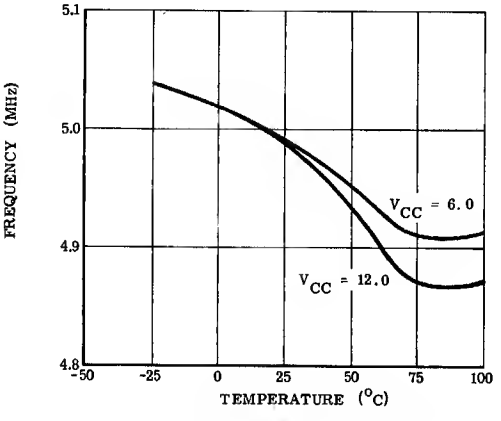


FIGURE 30 – FREQUENCY versus TEMPERATURE

The curves in Figure 29 shows the output voltage of the oscillator as a function of load resistance for various supply voltages. It is seen that for a load resistance greater than 10k ohms, the output voltage is essentially constant.

Figure 30 gives an indication of the frequency stability of this oscillator centered at 5.00 MHz at 25°C over a temperature range from -25°C to 100°C. Figure 31 is a photograph of the output waveform at 5.0 MHz.

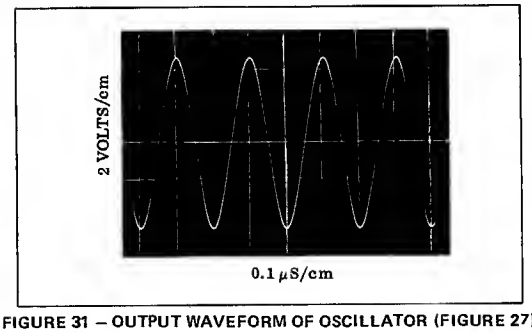


FIGURE 31 – OUTPUT WAVEFORM OF OSCILLATOR (FIGURE 27)

VIDEO AMPLIFIER

One of the many methods of using the MC1550 as a video amplifier as shown in Figure 32. The circuit may be analyzed for voltage gain using the equivalent circuit shown in Figure 33. Using model analysis, the equations from Figure 33 are:

$$\frac{e_S}{r_b' + R_S} = V_2\left(\frac{1}{\beta r_{e_1}} + \frac{1}{r_b' + R_S}\right) \tag{35}$$

$$0 = V_2\left(\frac{1}{r_{e_1}}\right) + V_3\left(\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}} + SC_S\right) \tag{36}$$

$$0 = -V_3\left(\frac{\alpha}{r_{e_1}}\right) + e_0\left(\frac{1}{R_L} + SC_O\right) \tag{37}$$

Where

$$\frac{1}{\beta} = \frac{1}{\beta_o} + \frac{S}{\omega_T}$$

and

$$C_O = C_S + C_L$$

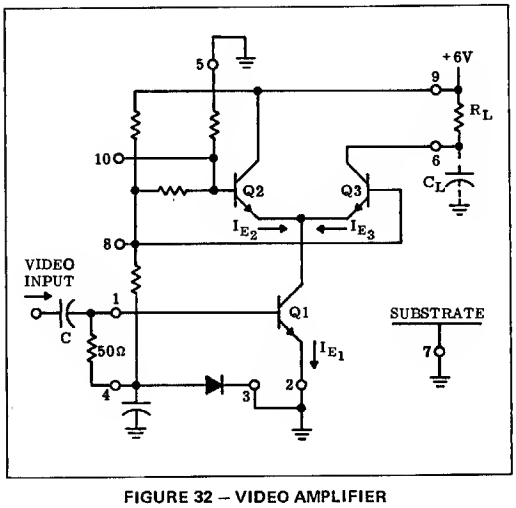


FIGURE 32 – VIDEO AMPLIFIER

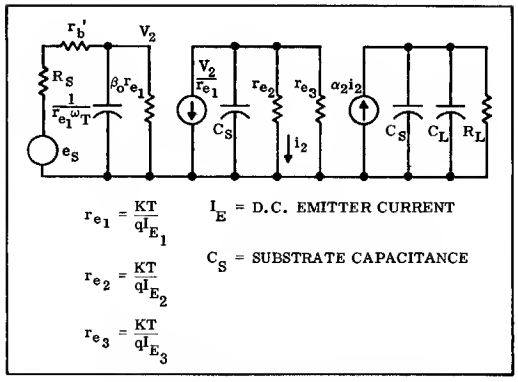


FIGURE 33 – MC1550 EQUIVALENT CIRCUIT

Using equations 35, 36, and 37 above, the equation for the voltage gain is

$$A_V(S) = \frac{e_o}{e_S} = -\frac{1}{r_b' + R_S}\left(\frac{\alpha}{r_{e_1} r_{e_2}}\right) \frac{1}{\left\{\left[\left(\frac{1}{r_{e_1}}\right)\left(\frac{1}{\beta_o} + \frac{S}{\omega_T}\right) + \frac{1}{r_b' + R_S}\right]\left[SC_S + \frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right]\left[SC_O + \frac{1}{R_L}\right]\right\}} \tag{38}$$

Equation 38 can be somewhat simplified if

$$\frac{1}{\beta_o r_{e_1}} \ll \frac{1}{r_b' + R_S} \quad \text{OR} \quad r_b' + R_S \ll \beta_o r_{e_1} \tag{39}$$

Using the simplification in Figure 5 and factoring, equation 40 results:

$$A_V(S) = -\frac{1}{r_b' + R_S}\left(\frac{\alpha}{r_{e_1} r_{e_2}}\right) \left[\frac{1}{\frac{C_S C_O}{r_{e_1}\omega_T}\left(S + \frac{r_{e_1}\omega_T}{r_b' + R_S}\right)\left(S + \frac{1}{C_S}\left[\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right]\right)\left(S + \frac{1}{R_L C_O}\right)}\right] \tag{40}$$

Using equation 40, the D.C. value of voltage gain is calculated by setting S = 0:

$$A_V(0) = -\frac{R_L}{r_{e_1} r_{e_2}\left(\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right)} \text{FOR } \alpha = 1 \tag{41}$$

Equation 41 clearly points out the effect that the AGC variations has on voltage gain. If V_{AGC} = 0 volts, then $I_{Q_3} \approx 0$ and $1/r_{e_3} \approx 0$. For this case, equation 41 becomes:

$$A_V(0) = -\frac{R_L}{r_{e_1}} \tag{41a}$$

If V_{AGC} = +6 volts, then $I_{Q_2} \approx 0$ and $1/r_{e_2} \approx 0$ or $r_{e_2} \to \infty$ so that equation 41 becomes

$$A_V(0) = -\frac{R_L}{r_{e_1}\left(1 + \frac{r_{e_2}}{r_{e_3}}\right)} \approx 0 \tag{42}$$

Equations 41a and 42 represent the extremes of the D.C. voltage gain, and equation 41 can be used to find the gain at any point between 0 and the maximum. Consider now the use of equation 40 in the design of a video amplifier to meet the following specifications:

$A_V(0) = 25$

$V_{CC} = 6$ volts

Bandwidth > 20 MHz

$R_S = 50$ ohms

The transistor parameters are

$r_b' = 50\Omega$

$\omega_T = 2\pi(9 \times 10^8)$ Hz

$C_S = 5$ pF

$r_{e_1} = 25\Omega$ For $V_{CC} = 6.0$ Volts

The load resistor, R_L required is:

$$R_L = A_V(0)\, r_{e_1}$$

$$R_L = 625\Omega.$$

The dominant pole will be created by the load capacitance and R_L. Since $C_S \approx 5$ pF, the value of C_L must be less than 8 pF for a bandwidth greater than 20 MHz. Therefore, assume that $C_O \approx 10$ pF, then the break frequencies are given by:

$$f_1 = \frac{1}{2\pi R_L C_O} = 25.4 \text{ MHz}$$

$$f_2 = \frac{r_{e_1} f_T}{r_b' + R_S} \approx \frac{f_T}{3} = 300 \text{ MHz}$$

$$f_3 = \frac{1}{C_S}\left(\frac{1}{r_{e_2}} + \frac{1}{r_{e_3}}\right) > 1.2 \text{ gHz for } V_{AGC} = 0 \text{ or } 6 \text{ volts.}$$

The curve in Figure 34 shows a comparison between measured and calculated data for the circuit of Figure 32 when $R_L = 625\Omega$ and $C_L < 5$ pF. The data indicates that, although a simplified model was used to analyze the circuit, reasonably valid results are obtained in the laboratory.

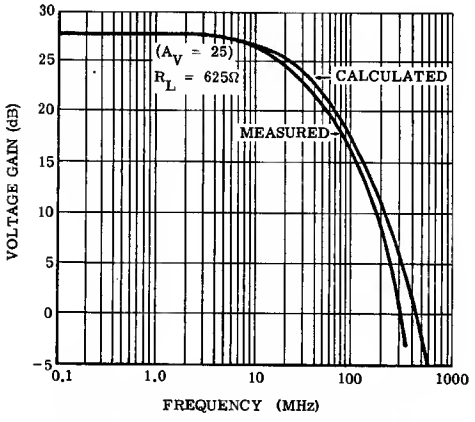


FIGURE 34 – MC1550 VIDEO AMPLIFIER GAIN versus FREQUENCY

AMPLITUDE MODULATOR

The AGC characteristics of the MC1550 make it very useful as an amplitude modulator as shown in Figure 35. If the voltage at the base of transistor Q_2 is time-varying, the gain of the amplifier will also be time-varying. By injecting an audio signal into the base of transistor Q_2, the RF carrier will be amplified as a function of the audio input. Considering the circuit in terms of y-parameters, the voltage gain is given by:

$$A_V = \frac{|y_{21}| \angle \phi}{y_{22} + Y_L} \qquad (43)$$

From this equation, it is seen that if $|y_{21}|$ is varied sinusoidally, the voltage gain varies sinusoidally, and the output will be an amplitude modulated wave. The amount of distortion will depend on how linear the gain varies with the input sinusoid. Figure 37 shows the manner in which $|y_{21}|$ varies with AGC voltage at 45 MHz ($V_{CC} = 6.0$V). The curve in Figure 37 shows that between $V_{AGC} = 2.75$ volts and $V_{AGC} = 4.25$ volts, $|y_{21}|$ is very linear with AGC voltage. By biasing the AGC line (pin 5) to 3.5 volts and impressing an audio signal on the base of Q_2 (pin 10), $|y_{21}|$ varies along the linear portion of the curve. Because of the linearity of this portion of the curve, very little distortion in the output results. Using the y-parameter curve of Figure 37, the up modulation and down modulation may be calculated. Referring to Figure 36, the up and down modulation factors are defined as:

$$M_u = \frac{E_{max} - E}{E} \quad \text{(UPWARD MODULATION)} \qquad (44)$$

$$M_d = \frac{E - E_{min}}{E} \quad \text{(DOWNWARD MODULATION)} \qquad (45)$$

Where:

E = peak amplitude of the unmodulated carrier

E_{max} = maximum amplitude attained by the modulated carrier envelope.

E_{min} = minimum amplitude of the modulated carrier envelope.

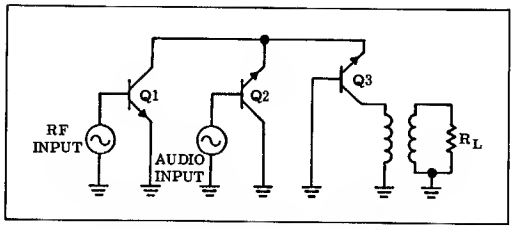


FIGURE 35 – SIMPLIFIED MODEL OF RF MODULATOR

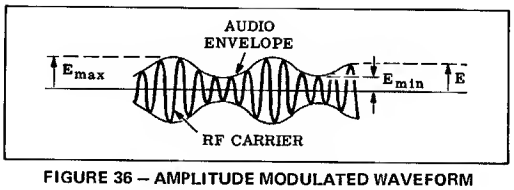


FIGURE 36 – AMPLITUDE MODULATED WAVEFORM

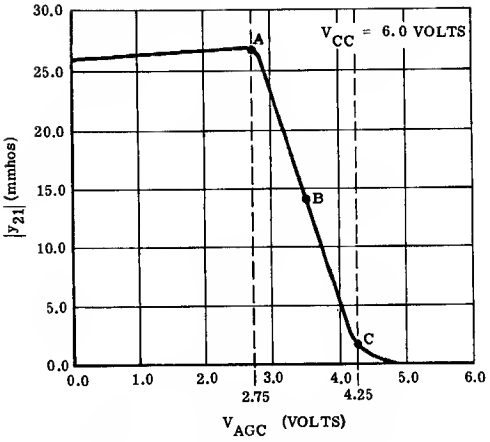


FIGURE 37 – $|y_{21}|$ versus V_{AGC} AT 45 MHz

Observe from Figure 37 that E_{max} occurs at point "A" where the audio signal is at minimum amplitude and E_{min} occurs at point "C" where the audio signal is at maximum amplitude. The nominal value of E occurs at point "B" when the audio signal crosses thru zero volts. If we let e_{in} be the input voltage, then the output voltage can be found from equation 43.

$$e_0 = \frac{e_{in}|y_{21}|}{y_{22} + Y_L} \tag{46}$$

Thus the values of E_{min}, E_{max}, and E can be found to be

$$E_{min} = \frac{e_{in}|y_{21}|_C}{y_{22} + Y_L} \tag{47}$$

$$E_{max} = \frac{e_{in}|y_{21}|_A}{y_{22} + Y_L} \tag{48}$$

$$E = \frac{e_{in}|y_{21}|_B}{y_{22} + Y_L} \tag{49}$$

$M\mu$ and M_d can now be found from equations 44 and 45:

$$M_u = \frac{|y_{21}|_A - |y_{21}|_B}{|y_{21}|_B} \tag{50}$$

and

$$M_d = \frac{|y_{21}|_B - |y_{21}|_C}{|y_{21}|_B} \tag{51}$$

Substituting the values of $|y_{21}|_A$, $|y_{21}|_B$ and $|y_{21}|_C$ found in Figure 37 into equations 51 and 52, we find,

$$M_u = 0.90$$
$$M_d = 0.91$$

These are the values of up modulation and down modulation which may be expected without distortion.

When the circuit shown in Figure 38 was designed and tested, the following results were achieved:

$$M_u = 0.89 \text{ and } M_d = 0.89$$

Two output waveforms of this modulator are shown in Figures 39(a) and 39(b). As one can see, very good modulation has been achieved with very little distortion.

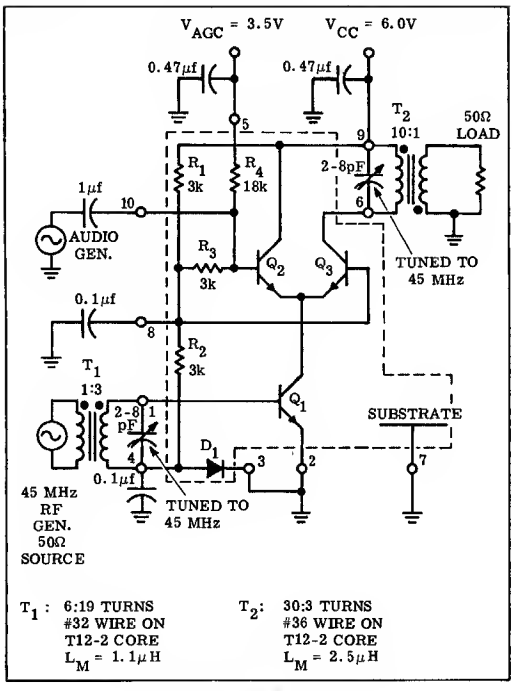
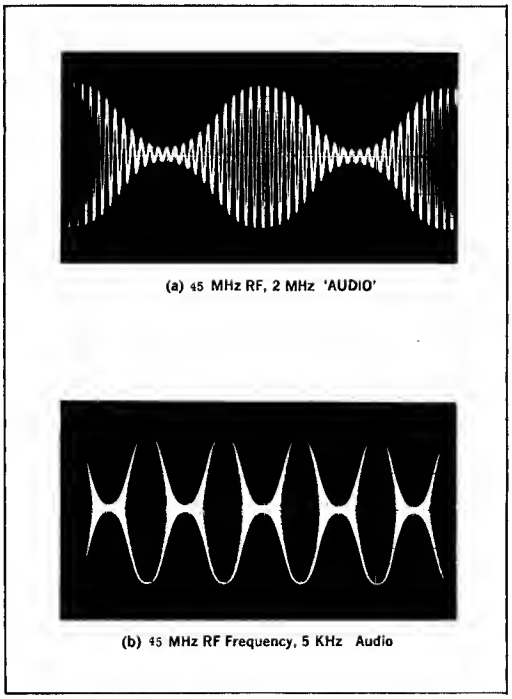


FIGURE 38 – RF MODULATOR



(a) 45 MHz RF, 2 MHz 'AUDIO'

(b) 45 MHz RF Frequency, 5 KHz Audio

FIGURE 39 – OUTPUT WAVEFORM OF RF MODULATOR (FIGURE 34)

APPENDIX A

For an ideal p-n junction, the current is related to the voltage by the equation

$$I = I_o\left(e^{\frac{V}{nV_T}} - 1\right) \tag{52}$$

where a positive value of V represents a forward biased junction, n is a parameter (≈2 for silicon) to account for recombination at the junction transition region, V_T is the electron-volt equivalent of temperature and is given by $V_T = KT/q$, and I_o is the reverse saturation current. Thus, for transistor Q_1 biasing

$$I_{D_1} = I_{o_{D_1}}\left(e^{\frac{V_{D_1}}{nV_T}} - 1\right) \text{and } I_{E_1} = I_{o_{E_1}}\left(e^{\frac{V_{BE}}{nV_T}} - 1\right). \tag{53}$$

When the diode is forward biased, V_{D_1} is equal to the base-emitter voltage, V_{BE}, of transistor Q_1 and the -1 term in the parenthesis can be neglected. Thus; we may write

$$I_{D_1} = I_{o_{D_1}}\left(e^{\frac{V}{nV_T}}\right) \text{and } I_{E_1} = I_{o_{E_1}}\left(e^{\frac{V}{nV_T}}\right) \tag{54}$$

where

$$V = V_{BE} = V_{D_1} .$$

If the two p-n junctions are physically matched by being located very close together, the reverse saturation currents will be nearly equal. That is,

$$I_{o_{D_1}} = I_{o_{E_1}} \tag{55}$$

thus, $I_{D_1} = I_{E_1}$ as given in the text.

APPENDIX B – TRANSITION WIDTH OF EMITTER-COUPLED CIRCUIT

The MC1550 is partially re-drawn in Figure 40. In this figure, Q_1 is represented as a current source and current I_3 is to be related to voltages V_8 and V_{10}:

The currents I_2 and I_e may be related to the voltages ϕ_1 and ϕ_2 by equations 56 and 57:

$$I_2 \approx a_{11}\, e^{\frac{q\phi_1}{KT}} \tag{56}$$

$$I_3 = a_{11}\, e^{\frac{q\phi_2}{KT}} \tag{57}$$

Assuming I_2 and I_3 are approximately equal to the emitter currents, then:

$$I_2 + I_3 = I_{Q_1} . \tag{58}$$

Also,

$$V_8 - V_{10} = \phi_1 - \phi_2 . \tag{59}$$

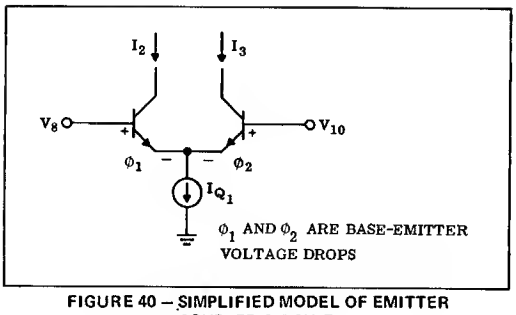


FIGURE 40 – SIMPLIFIED MODEL OF EMITTER COUPLED CIRCUIT

Using the above equations, the current I_3 may be found:

$$I_3 = \frac{I_{Q_1}}{1 + e^{\frac{q(V_8 - V_{10})}{KT}}} \tag{60}$$

Assuming V_{10} is held constant at some prescribed value, I_3 is plotted as a function of V_8 in Figure 41.

If $(V_8 - V_{10})$ is assumed to reach two values, one which causes $I_3 = 0.1\, I_{Q_1}$ (denote it as V_a) and one which causes $I_E = 0.9\, I_{Q_1}$ (denote it as V_b), then the difference between the two will give the transition width ΔV_B:

$$0.1\, I_{Q_1}\left(1 + e^{\frac{qV_a}{KT}}\right) = I_{Q_1} \tag{61}$$

$$0.9\, I_{Q_1}\left(1 + e^{\frac{qV_b}{KT}}\right) = I_{Q_1} \tag{62}$$

Solving for V_a and V_b we have

$$V_a = \left(\frac{KT}{q}\right) \ln 9 \tag{63}$$

$$V_b = \left(\frac{KT}{q}\right) \ln \frac{1}{9} . \tag{64}$$

Hence

$$\Delta V_8 = V_a - V_b \tag{65}$$

and

$$\Delta V_8 = \frac{KT}{q} \ln 9 + \frac{KT}{q} \ln 9 \tag{66}$$

or

$$\Delta V_8 = \frac{KT}{q} \ln 81 \approx 4.4\, \frac{KT}{q} . \tag{67}$$

At room temperature ($T \doteq 25^oC$)

$$\Delta V_8 = 114 \text{ mv} .$$

APPENDIX C – DERIVATION OF OSCILLATOR FREQUENCY AND THRESHOLD GAIN

The circuit shown in Figure 42 is an equivalent model of the transformer when the coefficient of coupling is not unity. The parameters for this model are as follows:

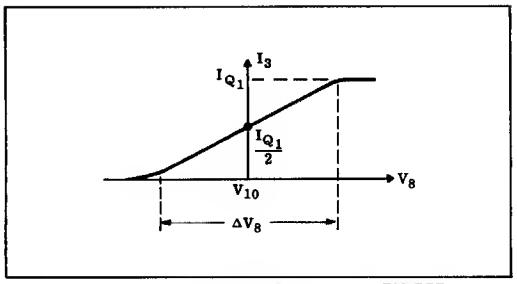


FIGURE 41 – TRANSITION WIDTH OF EMITTER COUPLED CIRCUIT

R_o = output resistance of the MC1550

R_L = external load resistance

R_1 = input resistance of the MC1550

C_o = output capacitance of the MC1550

C_L = external load capacitance

C_1 = input capacitance of the MC1550

L_e = leakage inductance of the transformer

$= (1 - K^2)\, L_p$

L_m = magnatizing inductance of the transformer

$= K^2 L_p$

L_p = primary inductance of transformer

L_s = secondary inductance of transformer

α = effective turns ratio $= K\sqrt{\frac{L_p}{L_s}}$

K = coefficient of coupling

In the circuit of Figure 43, the secondary impedance have been reflected into the primary and,

$$R_T = \frac{R_o R_L}{R_o + R_L},\quad R_X = \alpha^2 R_1,\quad C_T = C_o + C_L,\quad C_X = \frac{C_1}{\alpha^2}\ .$$

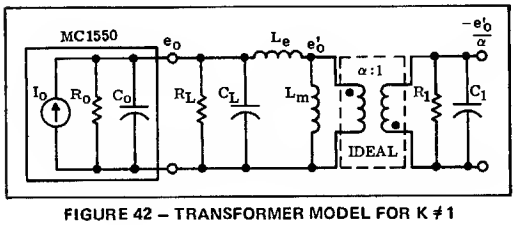


FIGURE 42 – TRANSFORMER MODEL FOR K ≠ 1

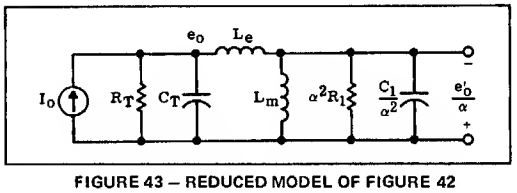


FIGURE 43 – REDUCED MODEL OF FIGURE 42

Consider next the output current of the MC1550 as an independent source and form a Thévenin equivalent for this source. This is shown in Figure 44. This is the figure which will be used for the following analysis. By definition,

$$\beta = \frac{e_1}{V_o} \tag{68}$$

or from Figure 40

$$\beta = \frac{-e'_o}{\alpha V_o}\ . \tag{69}$$

Solving for $\frac{e_o}{V_o}$ in Figure 25:

$$\frac{e'_o}{V_o} = \frac{S\left(S + \frac{1}{R_T C_T}\right)}{S^4(L_e C_X) + S^3\left(\frac{L_e}{R_X} + \frac{L_e C_X}{R_T C_T}\right) + S^2\left(1 + \frac{L_e}{L_m} + \frac{C_X}{C_T} + \frac{L_e}{R_T R_X C_T}\right)}$$

$$\frac{S\left(S + \frac{1}{R_T C_T}\right)}{+ S\left(\frac{1}{R_T C_T} + \frac{L_e}{L_m R_T C_T} + \frac{1}{R_X C_T}\right) + \frac{1}{L_m C_T}}\ . \tag{70}$$

Now letting $S = j\omega$

$$\frac{e'_o}{V_o} = \frac{-\omega^2 + j\omega\left(\frac{1}{R_T C_T}\right)}{\left[\omega^4\left(L_e C_X\right) - \omega^2\left(1 + \frac{L_e}{L_m} + \frac{C_X}{C_T} + \frac{L_e}{R_T R_X C_T}\right) + \frac{1}{L_m C_T}\right]}$$

$$\frac{-\omega^2 + j\omega\left(\frac{1}{R_T C_T}\right)}{- j\left[\omega^3\left(\frac{L_e}{R_X} + \frac{L_e C_X}{R_T C_T}\right) - \omega\left(\frac{1}{R_T C_T} + \frac{L_e}{L_m R_T C_T} + \frac{1}{R_X C_T}\right)\right]} \tag{71}$$

Multiplying both the numerator and denominator by the conjugate of the denominator, and setting the imaginary component equal to zero and combining like terms, we have

$$\omega^4 + \omega^2\left(\frac{R_X}{R_T}\right)\left(\frac{\frac{C_X}{C_T} - \frac{R_T}{R_X} + \frac{L_e}{R_T R_X C_T}}{L_e C_T}\right) - \frac{R_X}{R_T}\left(\frac{1}{L_m L_e C_T^2}\right) \tag{72}$$

The exact solution to this equation is quite complex and offers little insight to the analysis. However, with the following assumptions, this reduces to a very simple form.

Assume:

(A) $C_T \gg C_X$ (B) $\frac{L_e}{C_T} \ll R_T^2$ (C) $R_T \gg R_X$

For these assumptions,

$$\omega_o^2 = \frac{1}{L_e C_T} \tag{73}$$

or

$$f_o = \frac{1}{2\pi\sqrt{(1-K^2)\, L_P C_T}} \tag{74}$$

This is the approximate frequency of oscillation. To find the threshold gain of the amplifier, the value of ω_o found above must be substituted into the real component of β to solve for $\beta(\omega_o)$. With the same assumptions as above, this procedure results in equation 75:

$$\text{Real } \beta(\omega_o) = \frac{1 - \frac{L_e}{R_T C_T}\left[\frac{L_e}{L_m R_T} - \frac{1}{R_X}\right]}{-\alpha\left\{1 + \frac{L_e}{R_T C_T}\left[\frac{2}{R_X} + \frac{L_e}{R_T C_T R_X^2} - \frac{4R_T}{R_X^2}\right] - \frac{1 - \frac{L_e}{R_T C_T}\left[\frac{L_e}{L_m R_T} - \frac{1}{R_X}\right]}{\frac{4}{R_X}\left(\frac{L_e}{L_m} - 1\right) + \frac{1}{R_T}\left(\frac{L_e}{L_m} - 1\right)^2}\right\}} \tag{75}$$

which reduces to the approximation,

$$\text{Real } \beta(\omega_o) = -\frac{1}{\alpha} \tag{76}$$

The threshold gain, A_T, is now found from the equation

$$A_T(\omega_o) = \frac{1}{\beta(\omega_o)}$$

or

$$A_T(\omega_o) = -\alpha \tag{77}$$

where α is the effective coefficient of coupling.

Equations 74 and 77 are those given in the text.

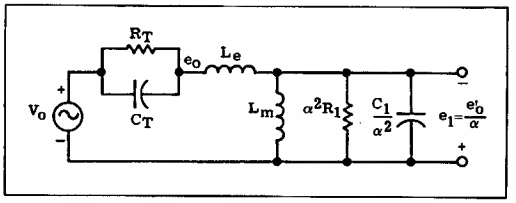


FIGURE 44 – THEVENIN EQUIVALENT OF FIGURE 43

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RF SMALL SIGNAL DESIGN USING ADMITTANCE PARAMETERS

INTRODUCTION

Design of the solid-state small-signal RF amplifier using two port parameters is a systematic, mathematical procedure, with an exact solution (free from approximation) available for the complete design problem. The only sources of error in the final design are parameter variations resulting from transistor parameter distributions and strays in the physical circuit. Parameter distributions result from limits in measurement and random variations among identically designed transistors.

The purpose of this paper is to provide, in a single working reference, the important relationships necessary for the complete solution of the RF small signal design problem using admittance parameters. Further, equations are given in the appendix for the conversion of other sets of two-port parameters to admittance parameters.

The paper is based on work by Linvill[1], Stern[2], and others. Those who may wish to consider the derivations of some of the expressions should refer to the original work presented in the references.

The report assumes that the reader is familiar with the two port parameter method of describing a linear active network. Several references are available on this subject.[1,2,6]

It has also been assumed that a suitable transistor for the task at hand has been selected, and that two-port parameters are available for the frequency and bias point which will be used. Device selection will not be covered as a separate topic in this report; rather, a thorough understanding of the material in the report should provide the designer with the tools he needs to select transistors for a particular small signal application.

The equations given in the text of the report are applicable to the common emitter, common base, or common collector configuration, if the applicable set of parameters (common emitter, common base, or common collector parameters) is used. Equations for the conversion of the admittance or hybrid parameters of any configuration to either of the other two configurations of the same parameter set are given in the appendix.

While directed primarily toward circuit design with conventional junction transistors, two port network theory has the advantage of being applicable to any linear active network. The same design approach and equations may therefore be used with field effect transistors[7], integrated circuits, or any other device which may be described as a linear active two-port network with measurable parameters.

Finally, various parameter interrelationships and other data are given in the Appendix.

GENERAL DESIGN CONSIDERATIONS

Design of the RF small signal tuned amplifier is usually based on a requirement for a specified power gain at a given frequency. Other design goals include bandwidth, stability, and input-output isolation. After a basic circuit type is selected, the applicable design equations can be solved.

Circuits may be categorized according to feedback (neutralization, unilateralization, or no feedback), and matching at transistor terminals (circuit admittances either matched or mismatched to transistor input and output admittances). Each of these circuit categories will be discussed, including the applicable design equations and the considerations leading to the selection of a particular configuration.

STABILITY

A major factor in the overall design is the potential stability of the transistor. This may be determined by computing the Linvill stability factor[1] C using the following expression: †

$$C = \frac{|y_{12}\, y_{21}|}{2g_{11}\, g_{22} - \mathrm{Re}\,(y_{12}y_{21})} \qquad (1)$$

When C is less than 1, the transistor is unconditionally stable. When C is greater than 1, the transistor is potentially unstable.

The C factor is a test for stability under a hypothetical worst case condition; that is, with both input and output transistor terminals open circuited. With no external feedback, an unconditionally stable transistor will not oscillate with any combination of source and load. If a transistor is potentially unstable, certain source and load combinations will produce oscillations.

Although the C factor may be used to determine the potential stability of a transistor, the conditions of open circuited source and load which are assumed in the C factor test are not applicable to a practical amplifier. Consequently it is also desirable to compute the relative stability of actual amplifier circuits, and Stern[2] has defined a stability factor k for this purpose. The k factor is similar to the C factor except that it also takes into account finite source and load admittances connected to the transistor. The expression for k is:

$$k = \frac{2\,(g_{11} + G_s)\,(g_{22} + G_L)}{|y_{12}y_{21}| + \mathrm{Re}\,(y_{12}y_{21})} \qquad (2)$$

If k is greater than one, the circuit will be stable. If k is less than one, the circuit will be potentially unstable and will very likely oscillate at some frequency.

Note that the C factor simply predicts potential stability of a transistor with an open circuited source and load, while the k factor provides a stability computation for a specific circuit.

Stability considerations will be discussed further in the descriptions of each basic circuit type to follow.

GENERAL DESIGN EQUATIONS

There are a number of design equations which are applicable to most types of amplifiers. These equations will be discussed first. Descriptions of specific amplifier types will then follow, and each will contain additional design equations applicable to that particular amplifier.

POWER GAIN

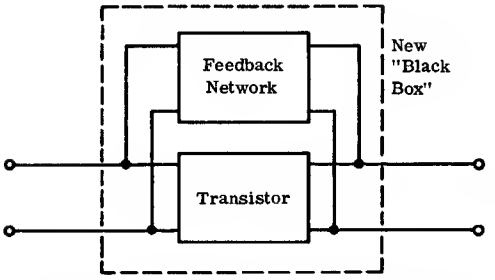
The general expression for power gain is:

$$G = \frac{|y_{21}|^2\, \mathrm{Re}\,(Y_L)}{\left|Y_L + y_{22}\right|^2 \mathrm{Re}\left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)} \qquad (3)$$

Equation 3 applies to circuits with no external feedback. It can also be used with circuits which have external feedback if the composite y parameters of both transistor and feedback network are substituted for the transistor y parameters in the equation. The composite y parameters

† $\mathrm{Re}\,(Y_{12}Y_{21})$ = Real part of $(Y_{12}Y_{21})$

are determined by considering the transistor and the feedback network to be two "black boxes" in parallel:



For example, the above combination of transistor and feedback network may be characterized as a single "black box" by the following equations:†

$$\begin{aligned} y_{11c} &= y_{11t} + y_{11f} \\ y_{12c} &= y_{12t} + y_{12f} \\ y_{21c} &= y_{21t} + y_{21f} \\ y_{22c} &= y_{22t} + y_{22f} \end{aligned} \qquad (4)$$

Where:

y_{11c}, y_{12c}, y_{21c}, y_{22c} are the composite y parameters of the parallel combination of transistor and feedback network.

y_{11t}, y_{12t}, y_{21t}, y_{22t} are the y parameters of the transistor.

y_{11f}, y_{12f}, y_{21f}, y_{22f} are the y parameters of the feedback network.

Note that, since this approach treats the transistor and feedback network combination as a single "black box" with y_{11c}, y_{12c}, y_{21c}, and y_{22c} as its y parameters, the composite y parameters may therefore be substituted in any of the design equations applicable to a linear, active, two port analysis.

The neutralized and unilateralized amplifiers are special cases of this general concept, and equations associated with those special cases will be given later.

Equation 3 provides a solution for power gain of the linear active network (transistor) only. Input and output networks are considered to be part of the source and load, respectively. Two important points should therefore be kept in mind:

(1) Power gain computed from equation 3 will not take into account network losses. Input network loss reduces power delivered to the transistor. Power lost in the output network is computed as useful power output, since the load admittance Y_L is the combination of the output network and its load.

(2) Power gain is independent of source admittance. An input mismatch results in less input power being delivered to the transistor. Accordingly, note that equation 3 does not contain the term Y_S.

†Refer to Seshu and Balabanian, "Linear Network Analysis, "John Wiley and Sons, 1959, P321

The power gain of a transistor together with its associated input and output networks may be computed by measuring the input and output network losses, and subtracting them from the power gain computed with equation 3 .

In some cases it may be desirable to include the effects of input matching in power gain computations. A convenient term is transducer gain G_T, defined as output power delivered to a load by the transistor, divided by the maximum input power available from the source.

The equation for transducer gain is:

$$G_T = \frac{4 \operatorname{Re}(Y_s) \operatorname{Re}(Y_L) |y_{21}|^2}{|(y_{11} + Y_s)(y_{22} + Y_L) - y_{12}y_{21}|^2} \qquad (5)$$

In this equation, Y_L is the composite transistor load admittance - composed of both output network and its load, and Y_S is the composite transistor source admittance - composed of both input network and its source. Therefore, transducer gain includes the effects of the degree of admittance match at the transistor input terminals but does not take into account input and output network losses.

As in equation 3 , the composite y parameters of a transistor feedback network combination may be substituted for the transistor y parameters when such a combination is used.

The Maximum Available Gain MAG is an often used transistor figure-of-merit. The MAG is the theoretical power gain of a transistor with its reverse transfer admittance y_{12} set equal to zero, and its source and load admittances conjugately matched to y_{11} and y_{22}, respectively.

If $y_{12} = 0$, the transistor exhibits an input admittance equal to y_{11} and an output admittance equal to y_{22}.† The equation for MAG is, therefore, obtained by solving the general power gain expression, equation 3 , with the conditions

$$y_{12} = 0$$

$$y_L = y_{22}^*$$

$$\text{and } y_s = y_{11}^*$$

which yields:

$$MAG = \frac{|y_{21}|^2}{4 \operatorname{Re}(y_{11}) \operatorname{Re}(y_{22})} \qquad (6)$$

MAG is a figure of merit only, since it is physically impossible to reduce y_{12} to zero without changing the other parameters of the transistor. An external feedback network may be used to achieve a composite y_{12} of zero, but then the other composite parameters will also be modifed according to the relationships given in the discussion of the composite transistor - feedback network "black box."

TRANSISTOR INPUT AND OUTPUT ADMITTANCES

The expression for the input admittance of a transistor is:

$$Y_{IN} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L} \qquad (7)$$

†Obtained by solving the equations for transistor Y_{IN} and Y_{OUT} with y_{12} equal to zero. These equations are given later in the report.

The expression for the output admittance of a transistor is:

$$Y_{OUT} = y_{22} - \frac{y_{12}\, y_{21}}{y_{11} + Y_s} \qquad (8)$$

When the feedback parameter y_{12} is not zero, Y_{IN} is dependent on load admittance and Y_{OUT} is dependent on source admittance.

AMPLIFIER STABILITY

One of the major considerations in RF amplifier design is stability. The stability of a final design can be assured by including stability computations and considering stability in all design decisions relating to feedback and transistor source and load admittances.

The potential stability of the transistor should first be computed using equation 1 .

The various alternatives concerning input - output matching and neutralization - unilateralization will now be discussed for both the unconditionally stable transistor and the potentially unstable transistor.

THE UNCONDITIONALLY STABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is less than one, the transistor is unconditionally stable. Oscillations will not occur using any combination of source and load admittances without external feedback. Stability is therefore eliminated as a factor in the remainder of the design, and complete freedom is possible with regard to matching and neutralization to optimize the amplifier for other performance requirements.

AMPLIFIERS WITHOUT FEEDBACK

The amplifier with no feedback is a logical choice for the unconditionally stable transistor in many applications since it may offer the advantages of fewer components and a simple tuning procedure.

Source and load admittances may be selected for maximum gain and/or any number of other requirements. Power gain and transducer gain may be computed using equations 3 and 5 , respectively; input and output admittances may be computed using equations 7 and 8, respectively.

The amplifier stability factor may be computed using equation 2 . While amplifier stability was assured from the beginning by the use of an unconditionally stable transistor, the designer may still wish to perform this computation to provide some insight into danger of instability under adverse environmental conditions, source and load variations, etc.

G_{max}

G_{max}, the highest transducer gain possible without external feedback, forms a special case of the no feedback amplifier.

The source and load admittances required to achieve G_{max} may be computed from the following:

$$G_s = \frac{1}{2\ \mathrm{Re}(y_{22})} \left\{ \left[2\ \mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}} \qquad (9)$$

$$B_s = -\mathrm{Im}(y_{11}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{22})} \qquad (10)$$

$$G_L = \frac{1}{2\ \mathrm{Re}(y_{11})} \left\{ \left[2\ \mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}} \qquad (11)$$

$$B_L = -\mathrm{Im}(y_{22}) + \frac{\mathrm{Im}(y_{21}y_{12})}{2\ \mathrm{Re}(y_{11})} \qquad (12)$$

Therefore, if the maximum possible power gain without feedback is desired for an amplifier, equations 9, 10, 11, and 12 are used to compute Y_S and Y_L.

The magnitude of G_{max} may be computed from the following expression:

$$G_{max} = \frac{|y_{21}|^2}{2\ \mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) + \left\{ \left[2\ \mathrm{Re}(y_{11})\,\mathrm{Re}(y_{22}) - \mathrm{Re}(y_{12}y_{21}) \right]^2 - \left| y_{12}y_{21} \right|^2 \right\}^{\frac{1}{2}}} \qquad (13)$$

Equations 9, 10, 11, and 12 can be obtained by differentiating equation 5 with respect to G_S, B_S, G_L, and B_L, and setting the four derivatives equal to zero. The G_S, B_S, G_L, and B_L thus computed can then be substituted in equation 5 to obtain the expression for G_{max}, equation 13.

THE LINVILL METHOD

The amplifier without feedback design problem may also be solved graphically using a technique developed by J.G. Linvill.† Linvill's technique is very useful for a certain class of problems. Since it is so fully discussed in many good references we will not go into it further here. An advantage of the Linvill technique is that it provides a reasonably rapid graphic solution relating gain, bandwidth, and stability. A disadvantage is its scope of usefulness, since the standard Linvill solution applies only to an amplifier with no external feedback and with Y_S conjugately matched to the transistor input admittance, Y_{IN}.

THE UNILATERALIZED AMPLIFIER

Unilateralization consists of employing an external feedback network to achieve a composite y_{12} of zero.

While unilateralization is perhaps most often used to achieve stability with a potentially unstable transistor, other circuit considerations may also warrant the use of unilateralization with the unconditionally stable transistor. For example, the input-output isolation afforded by unilateralization may be desirable in a particular design.

Design equations for the unilateralized case are obtained by first computing the composite y parameters of the transistor - feedback network combination and then substituting the composite parameters in the general equations.

Referring to the discussion on composite y parameters and setting up the basic condition that y_{12c} must equal zero, the other composite y parameters can be computed. Assuming that a passive feedback network is being used, then

$$y_{11f} = y_{22f} = -y_{12f} = -y_{21f},$$

and since $y_{12c} = 0$, $y_{12t} + y_{12f} = 0$

then $y_{12t} = -y_{12f}$,

and $y_{12t} = -y_{12f} = y_{11f} = y_{22f} = -y_{21f}$

†Application Note AN166.
See also reference 5 in the bibliography.

Substituting the above results in equations 4 yields the following:

$$y_{11c} = y_{11t} + y_{12t}$$

$$y_{22c} = y_{22t} + y_{12t}$$

$$y_{12c} = y_{12t} - y_{12t} = 0$$

$$y_{21c} = y_{21t} - y_{12t}$$

Substituting these composite y parameters in equations 7, 8, 3, 16, and 5 respectively, yields equations 14, 15, 16, 17 and 18 for the unilateralized case:

Unilateralized input admittance

$$Y_{IN} = y_{11} + y_{12} \tag{14}$$

Unilateralized output admittance

$$Y_{OUT} = y_{22} + y_{12} \tag{15}$$

Unilateralized power gain, general expression:

$$G_{PU} = \frac{\left|y_{21} - y_{12}\right|^2 \operatorname{Re}(Y_L)}{\left|Y_L + y_{22} + y_{12}\right|^2 \operatorname{Re}(y_{11})} \tag{16}$$

Unilateralized power gain with Y_L conjugately matched to Y_{OUT}:

$$G_U = \frac{\left|y_{21} - y_{12}\right|^2}{4 \operatorname{Re}(y_{11} + y_{12}) \operatorname{Re}(y_{22} + y_{12})} \tag{17}$$

Unilateralized transducer gain:

$$G_{TU} = \frac{4 \operatorname{Re}(Y_S) \operatorname{Re}(Y_L) \left|y_{21} - y_{12}\right|^2}{\left|(y_{11} + y_{12} + Y_S)(y_{22} + y_{12} + Y_L)\right|^2} \tag{18}$$

Note that equations 14, 15, 16, 17, and 18, are given entirely in terms of the transistor y parameters, not those of the feedback network or the composite.

Another benefit of unilateralization is input - output isolation. As can be seen in equations 14 and 15, Y_{IN} is completely independent of Y_L, and Y_{OUT} is similarly independent of Y_S. In a practical sense, this means that in a single or multi-stage amplifier using unilateralized stages, tuning of any one network will not affect tuning in other parts of the circuit. Thus, the troublesome task of having to re-peak an entire amplifier following a change in tuning at a single point can be eliminated.

NEUTRALIZATION

Neutralization consists of employing a feedback network to reduce y_{12} to some value other than zero. Neutralization is generally used for the same purposes as unilateralization, but provides something less than the ideal cancellation of the transistor feedback parameter which unilateralization achieves. A typical example of neutralization might be a feedback network which provides a composite b_{12} of zero while having only a negligible effect on the transistor g_{12}.

The equations for a particular neutralized case would be developed in the same manner as those for the unilateralized case. Since there are an infinite number of possibilities, no specific equations will be given here.

This completes the discussion of design with the unconditionally stable transistor. The potentially unstable transistor will now be considered.

THE POTENTIALLY UNSTABLE TRANSISTOR

When the Linvill stability factor of the transistor as determined by equation 1 is greater than one, the transistor is potentially unstable. Certain combinations of source and load admittances will cause oscillations if no feedback is used. In designing with the potentially unstable transistor, steps must be taken to insure that the amplifier will be stable.

Stability is usually achieved by one or both of two methods:

(1) Using a feedback network which reduces the composite y_{12} to a value which insures stability.

(2) Choosing a source and load admittance combination which provides stability.

A discussion of these basic methods is given below.

USING FEEDBACK TO ACHIEVE STABILITY

Either unilateralization or neutralization may be used to achieve stability. If unilateralization is used, the transistor-feedback network combination will be unconditionally stable. This may be verified by computing the Linvill stability factor of the combination. Since $y_{12c} = 0$, the numerator in equation 1 would be zero.

With stability thus assured, the remainder of the design may then be done to satisfy other requirements placed on the amplifier. After unilateralization has converted the potentially unstable transistor to an unconditionally stable combination, all other aspects of the design are identical to the unilateralized case with the unconditionally stable transistor. Power gains and input and output admittances may be computed using equations 14 through 18.

If neutralization is used to achieve stability, the Linvill stability factor can be used to compute the potential stability of any transistor - neutralization-network combination. Since in this case $y_{12c} \neq 0$, C will have a value other than zero.

After unconditional stability of the transistor-neutralization network combination has been achieved, the design may then be completed by treating the combination as an unconditionally stable transistor, and proceeding with the case of the unconditionally stable transistor in an amplifier without feedback. Power gains, input and output admittances, and the circuit stability factor may be computed by using the composite parameters of the combination in equations 2, 3, 5, 7, and 8.

STABILITY WITHOUT FEEDBACK

A stable design with the potentially unstable transistor is possible without external feedback by proper choice of source and load admittances. This can be seen by inspection of equation 2; G_S and/or G_L can be made large enough to yield a stable circuit regardless of the degree of potential instability of the transistor.

This suggests a relatively simple way to achieve a stable design with a potentially unstable transistor. A circuit stability factor k is selected, and equation 2 is used to arrive at values of G_S and G_L which will provide the desired k. In achieving a particular circuit stability factor, the designer may choose any of the following combinations of matching or mismatching of G_S and G_L to the transistor input and output conductances, respectively:

(1) G_S matched and G_L mismatched

(2) G_L matched and G_S mismatched

(3) Both G_S and G_L mismatched

Often a decision on which combination to use will be dictated by other performance requirements or practical considerations.

Once G_S and G_L have been chosen, the remainder of the design may be completed using the relationships which apply to the amplifier without feedback. Power gain and input and output admittances may be computed using equations 3, 5, 7, and 8.

Although the above procedure may be adequate in many cases, a more systematic method of source and load admittance determination is desirable for designs which demand maximum power gain per degree of circuit stability. Stern has analyzed this problem and developed equations for computing the conductance and susceptance of both Y_S and Y_L for maximum power gain for a particular circuit stability factor.[2,4] These equations are given here:

$$G_S = \sqrt{\frac{k\left(\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right)}{2}} \cdot \sqrt{\frac{g_{11}}{g_{22}}} - g_{11} \tag{19}$$

$$G_L = \sqrt{\frac{k\left(\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right)}{2}} \cdot \sqrt{\frac{g_{22}}{g_{11}}} - g_{22} \tag{20}$$

$$B_S = \frac{(G_S + g_{11})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{11} \tag{21}$$

$$B_L = \frac{(G_L + g_{22})\ Z_o}{\sqrt{k\left[\left|y_{12}y_{21}\right| + \mathrm{Re}(y_{12}y_{21})\right]}} - b_{22} \tag{22}$$

Where,

$$Z = \frac{(B_S + b_{11})(G_L + g_{22}) + (B_L + b_{22})\,k(L+M)/2(G_L + g_{22})}{\sqrt{k\ (L + M)}} \tag{23}$$

$$L = \left|y_{12}y_{21}\right| \tag{24}$$

$$M = \mathrm{Re}(y_{12}y_{21}) \tag{25}$$

Defining D as the denominator in equation 5 yields:

$$D = \frac{Z^4}{4} + \frac{\left[k(L + M) + 2M\right] Z^2}{2} - 2NZ\sqrt{k(L + M)} + A^2 + N^2 \tag{26}$$

where,

$$A = \frac{k(L + M)}{2} - M, \tag{27}$$

$$N = \mathrm{Im}(y_{12}y_{21}), \tag{28}$$

and,

Z_o = that real value of Z which results in the smallest minimum of D, found by setting,

$$\frac{dD}{dZ} = Z^3 + \left[k(L + M) + 2M\right] Z - 2N\sqrt{k(L + M)}. \tag{29}$$

equal to zero.

Computation of Y_S and Y_L using equations 19 through 29 is a bit tedious to be done very frequently, and this may have discouraged wide usage of the complete Stern solution. However, examination of Stern's work suggests some interesting shortcuts:

(A) COMPUTATION OF G_S AND G_L ONLY, USING EQUATIONS 19 AND 20. If a value equal to $-b_{22}$ is then chosen for B_L, the resulting Y_L will be very close to the true Y_L for maximum gain. The transistor Y_{IN} can then be computed from Y_L using equation 7, and B_S can be set equal to $-\mathrm{Im}(Y_{IN})$.

Computation of B_S and B_L comprise by far the more complex portion of the Stern solution. This alternate method therefore permits the designer to closely approximate the exact Stern solution for Y_S and Y_L while avoiding that portion of the computations which are the most complex and time consuming. Further, the circuit can be designed with tuning adjustments for varying B_S and B_L, thereby creating the possibility of experimentally achieving the true B_S and B_L for maximum gain as accurately as if all the Stern equations had been solved.

(B) MISMATCHING G_S TO g_{11} AND G_L TO g_{22} BY AN EQUAL RATIO YIELDS A TRUE STERN SOLUTION FOR G_S AND G_L. This can be derived from equations 19 and 20, which lead to the following result:

$$\frac{G_L}{g_{22}} = \frac{G_S}{g_{11}} \tag{30}$$

If a mismatch ratio, R, is defined as follows,

$$R = \frac{G_L}{g_{22}} = \frac{G_S}{g_{11}} \tag{31}$$

then R may be computed for any particular circuit stability factor using the equation:

$$(1 + R)^2 = k\left[\frac{\left|y_{21}y_{12}\right| + \mathrm{Re}(y_{12}y_{21})}{2\ g_{11}\ g_{22}}\right] \tag{32}$$

Equation 32 was derived from equations 2 and 31. Having thus determined R, G_S and G_L can be quickly found using equation 31.

B_S and B_L can then be determined in the manner described above in alternate method (A).

This alternate method may be advantageous if source and load admittances and power gains for several different values of k are desired. Once the R for a particular k has been determined, the R for any other k may be quickly found from the equation

$$\frac{(1 + R_1)^2}{(1 + R_2)^2} = \frac{k_1}{k_2} \tag{33}$$

where R_1 and R_2 are values of R corresponding to k_1 and k_2, respectively.

(C) COMPUTER DESIGN. The complete Stern design problem may be programmed into a computer. Power gain, circuit stability factor, Y_S and Y_L can be obtained from the computer for any value of k. MAG, G_U, and the Linvill stability factor of the transistor may also be included in the program.

After employing either the complete Stern solution or an alternate method to obtain Y_S and Y_L for the potentially unstable transistor in an amplifier without feedback, power gains and input and output admittances may be obtained using equations 3, 5, 7, and 8.

SENSITIVITY

In all but the unilateralized amplifier, Y_{IN} is a function of load admittance. Thus Y_{IN} changes with output circuit tuning, and this can be troublesome. Consequently, it is sometimes desirable to compute the extent of variation of Y_{IN} with changes in Y_L. A term, sensitivity δ, has been defined to provide a measure of this characteristic, and is equal to per cent change in Y_{IN} divided by per cent change in Y_L. The equation for sensitivity is:

$$\delta = \left|\frac{Y_L}{y_{22} + Y_L}\right| \cdot \left|\frac{g_{11}}{y_{11}}\right| \cdot \frac{K}{\left|\frac{y_{22} + Y_L}{g_{22}} + \frac{g_{11}}{y_{11}}\ K\ e^{j\theta}\right|} \tag{34}$$

where,

$$K = \left|\frac{y_{21}\ y_{12}}{g_{11}\ g_{22}}\right|$$

$$\theta = \arg\ (-y_{12}y_{21}) +$$

$$K\ e^{j\theta} = K\ (\cos\theta + j\ \sin\theta)$$

A more complete discussion of sensitivity is given in reference 6.

SUMMARY

The small signal amplifier performance of a transistor is completely described by two port admittance parameters. Based on these parameters, equations for computing the stability, gain, and optimum source and load admittances for the unilateralized, neutralized, and no-feedback amplifier cases have been discussed.

The unconditionally stable transistor will not oscillate with any combination of source and load admittances, and circuits using a stable transistor may be optimized for other performance requirements without fear of oscillations.

The potentially unstable transistor requires that steps be taken to guarantee a stable design. Stability is usually achieved by unilateralization, neutralization, or selection of source and load admittances which result in a stable amplifier.

Unilateralization and neutralization reduce the composite reverse transfer admittance. They may be used to achieve stability, input - output isolation, or both.

Maximum power gain per degree of circuit stability without feedback may be achieved using Stern's equations.

The degree of input - output isolation is described by the term sensitivity, which makes it possible to compute changes in input admittance for any change in load admittance.

The theory and design equations in this report are applicable to any linear active device which may be characterized as a two-port network. Therefore, the term "transistor" used herein refers generally to all such devices, including FETs and integrated circuits.

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GLOSSARY

C	=	Linvill's stability factor
k	=	Stern's stability factor
G_s	=	Real part of the source admittance
G_L	=	Real part of the load admittance
B_s	=	Imaginary part of the source admittance
B_L	=	Imaginary part of the load admittance
g_{11}	=	Real part of y_{11}
g_{22}	=	Real part of y_{22}
G	=	Generalized power gain
Y_L	=	Complex load admittance
Y_s	=	Complex source admittance
G_T	=	Transducer gain
MAG	=	Maximum available gain
*	=	Conjugate
Y_{IN}	=	Input admittance
Y_{OUT}	=	Output admittance
G_{max}	=	Maximum gain without feedback
G_U	=	Unilateralized gain
G_{TU}	=	Unilateralized transducer gain
δ	=	Sensitivity

APPENDIX I

A. Conversions among parameter types for y, z, h, and g parameters.

h to y

$$y_{11} = \frac{1}{h_{11}} \qquad y_{12} = \frac{-h_{12}}{h_{11}} \qquad y_{21} = \frac{h_{21}}{h_{11}} \qquad y_{22} = \frac{\Delta h}{b_{11}}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

y to h

$$h_{11} = \frac{1}{y_{11}} \qquad h_{12} = \frac{-y_{12}}{y_{11}} \qquad h_{21} = \frac{y_{21}}{y_{11}} \qquad h_{22} = \frac{\Delta y}{y_{11}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

h to z

$$z_{11} = \frac{\Delta h}{h_{22}} \qquad z_{12} = \frac{h_{12}}{h_{22}} \qquad z_{21} = \frac{-h_{21}}{h_{22}} \qquad z_{22} = \frac{1}{h_{22}}$$

z to h

$$h_{11} = \frac{\Delta z}{z_{22}} \qquad h_{12} = \frac{z_{12}}{z_{22}} \qquad h_{21} = \frac{-z_{21}}{z_{22}} \qquad h_{22} = \frac{1}{z_{22}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

h to g

$$g_{11} = \frac{h_{22}}{\Delta b} \qquad g_{12} = \frac{-h_{12}}{\Delta h} \qquad g_{21} = \frac{-h_{21}}{\Delta h} \qquad g_{22} = \frac{h_{11}}{\Delta h}$$

where $\Delta h = h_{11} h_{22} - h_{12} h_{21}$

g to h

$$h_{11} = \frac{g_{22}}{\Delta g} \qquad h_{12} = \frac{-g_{12}}{\Delta g} \qquad h_{21} = \frac{-g_{21}}{\Delta g} \qquad h_{22} = \frac{g_{11}}{\Delta g}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

z to y

$$y_{11} = \frac{z_{22}}{\Delta z} \qquad y_{12} = \frac{-z_{12}}{\Delta z} \qquad y_{21} = \frac{-z_{21}}{\Delta z} \qquad y_{22} = \frac{z_{11}}{\Delta z}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

y to z

$$z_{11} = \frac{y_{22}}{\Delta y} \qquad z_{12} = \frac{-y_{12}}{\Delta y} \qquad z_{21} = \frac{-y_{21}}{\Delta y} \qquad z_{22} = \frac{y_{11}}{\Delta y}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

z to g

$$g_{11} = \frac{1}{z_{11}} \qquad g_{12} = \frac{-z_{12}}{z_{11}} \qquad g_{21} = \frac{z_{21}}{z_{11}} \qquad g_{22} = \frac{\Delta z}{z_{11}}$$

where $\Delta z = z_{11} z_{22} - z_{12} z_{21}$

g to z

$$z_{11} = \frac{1}{g_{11}} \qquad z_{12} = \frac{-g_{12}}{g_{11}} \qquad z_{21} = \frac{g_{21}}{g_{11}} \qquad z_{22} = \frac{\Delta g}{g_{11}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

g to y

$$y_{11} = \frac{\Delta g}{g_{22}} \qquad y_{12} = \frac{g_{12}}{g_{22}} \qquad y_{21} = \frac{-g_{21}}{g_{22}} \qquad y_{22} = \frac{1}{g_{22}}$$

where $\Delta g = g_{11} g_{22} - g_{12} g_{21}$

y to g

$$g_{11} = \frac{\Delta y}{y_{22}} \qquad g_{12} = \frac{y_{12}}{y_{22}} \qquad g_{21} = \frac{-y_{21}}{y_{22}} \qquad g_{22} = \frac{1}{y_{22}}$$

where $\Delta y = y_{11} y_{22} - y_{12} y_{21}$

B. Conversions among common emitter, common base, and common collector parameters of the same type for y, and h parameters.

Common emitter y parameters in terms of common base and common collector y parameters.

$$y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b} = y_{11c}$$

$$y_{12e} = -(y_{12b} + y_{22b}) = -(y_{11c} + y_{12c})$$

$$y_{21e} = -(y_{21b} + y_{22b}) = -(y_{11c} + y_{21c})$$

$$y_{22e} = y_{22b} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common base y parameters in terms of common emitter and common collector y parameters.

$$y_{11b} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{22c}$$

$$y_{12b} = -(y_{12e} + y_{22e}) = -(y_{21c} + y_{22c})$$

$$y_{21b} = -(y_{21e} + y_{22e}) = -(y_{12c} + y_{22c})$$

$$y_{22b} = y_{22e} = y_{11c} + y_{12c} + y_{21c} + y_{22c}$$

Common collector y parameters in terms of common emitter and common base y parameters.

$$y_{11c} = y_{11e} = y_{11b} + y_{12b} + y_{21b} + y_{22b}$$

$$y_{12c} = -(y_{11e} + y_{12e}) = -(y_{11b} + y_{21b})$$

$$y_{21c} = -(y_{11e} + y_{21e}) = -(y_{11b} + y_{12b})$$

$$y_{22c} = y_{11e} + y_{12e} + y_{21e} + y_{22e} = y_{11b}$$

Common emitter h parameters in terms of common base and common collector h parameters.

$$h_{11e} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11c}$$

$$h_{12e} = \frac{h_{11b} h_{22b} - h_{12b}(1+h_{21b})}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{11b} h_{22b}}{1 + h_{21b}} - h_{12b} = 1-h_{12c}$$

$$h_{21e} = \frac{-h_{21b}(1-h_{12b}) - h_{22b} h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{-h_{21b}}{1 + h_{21b}} = -(1 + h_{21c})$$

$$h_{22e} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b} h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22c}$$

Common base h parameters in terms of common emitter and common collector h parameters.

$$h_{11b} = \frac{h_{11e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} b_{22e}} \approx \frac{h_{11e}}{1 + h_{21e}}$$

$$= \frac{h_{11c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-h_{11c}}{h_{21c}}$$

$$h_{12b} = \frac{h_{11e} b_{22e} - h_{12e}(1 + h_{21e})}{(1 + b_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{b_{11e} h_{22e}}{1 + h_{21e}} - h_{12e}$$

$$= \frac{h_{21c}(1-h_{12c}) + h_{11c} b_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx (h_{12c} - 1) - \frac{b_{11c} b_{22c}}{h_{21c}}$$

$$h_{21b} = \frac{-h_{21e}(1-h_{12e}) - h_{11e} h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{-h_{21e}}{1 + h_{21e}}$$

$$= \frac{h_{12c}(1 + h_{21c}) - h_{11c} h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{-(1 + h_{21c})}{h_{21c}}$$

$$h_{22b} = \frac{h_{22e}}{(1 + h_{21e})(1-h_{12e}) + h_{11e} h_{22e}} \approx \frac{h_{22e}}{1 + h_{21e}}$$

$$= \frac{h_{22c}}{h_{11c} h_{22c} - h_{21c} h_{12c}} \approx \frac{h_{22c}}{h_{21c}}$$

Common collector h parameters in terms of common base and common emitter h parameters.

$$h_{11c} = \frac{h_{11b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\, h_{11b}} \approx \frac{h_{11b}}{1 + h_{21b}} = h_{11e}$$

$$h_{12c} = \frac{1 + h_{21b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\, h_{11b}} \approx 1 = 1-h_{12e}$$

$$h_{21c} = \frac{h_{12b} - 1}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\, h_{11b}} \approx \frac{-1}{1 + h_{21b}} = -(1 + h_{21e})$$

$$h_{22c} = \frac{h_{22b}}{(1 + h_{21b})(1-h_{12b}) + h_{22b}\, h_{11b}} \approx \frac{h_{22b}}{1 + h_{21b}} = h_{22e}$$

Expressions for voltage gain, current gain, input impedance, and output impedance in terms of y, z, h, and g parameters.

Voltage Gain

$$A_v = \frac{z_{21}\, Z_L}{\Delta z + z_{11}\, Z_L} = \frac{-y_{21}}{y_{22} + Y_L} = \frac{-h_{21}\, Z_L}{h_{11} + \Delta h Z_L} = \frac{g_{21}\, Z_L}{g_{22} + Z_L}$$

Current Gain

$$A_i = \frac{-z_{21}}{z_{22} + Z_L} = \frac{-y_{21}\, Y_L}{\Delta y + y_{11}\, Y_L} = \frac{-h_{21}\, Y_L}{h_{22} + Y_L} = \frac{-g_{21}}{\Delta g + g_{11}\, Z_L}$$

Input Impedance

$$Z_{IN} = \frac{\Delta z + z_{11}\, Z_L}{z_{22} + Z_L} = \frac{y_{22} + Y_L}{\Delta y + y_{11}\, Y_L} = \frac{\Delta h + h_{11}\, Y_L}{h_{22} + Y_L} = \frac{g_{22} + Z_L}{\Delta g + g_{11}\, Z_L}$$

Output Impedance

$$Z_{OUT} = \frac{\Delta z + z_{22}\, Z_s}{z_{11} + Z_s} = \frac{y_{11} + Y_s}{\Delta y + y_{22}\, Y_s} = \frac{h_{11} + Z_s}{\Delta h + h_{22}\, Z_s} = \frac{\Delta g + g_{22}\, Y_s}{g_{11} + Y_s}$$

Conversion between y parameters and s (scattering) parameters:

$$s_{11} = \frac{(1-y_{11})(1+y_{22}) + y_{12}\, y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}\, y_{21}} \dagger$$

$$s_{12} = \frac{-2y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}\, y_{21}} \dagger$$

$$s_{21} = \frac{-2y_{21}}{(1+y_{11})(1+y_{22}) - y_{12}\, y_{21}} \dagger$$

$$s_{22} = \frac{(1+y_{11})(1-y_{22}) + y_{21}\, y_{12}}{(1+y_{11})(1+y_{22}) - y_{12}\, y_{21}} \dagger$$

$$y_{11} = \left[\frac{(1+s_{22})(1-s_{11}) + s_{12}\, s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}\, s_{21}}\right] \frac{1}{Z_o}$$

$$y_{12} = \left[\frac{-2s_{12}}{(1+s_{11})(1+s_{22}) - s_{12}\, s_{21}}\right] \frac{1}{Z_o}$$

$$y_{21} = \left[\frac{-2s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}\, s_{21}}\right] \frac{1}{Z_o}$$

$$y_{22} = \left[\frac{(1+s_{11})(1-s_{22}) + s_{12}\, s_{21}}{(1+s_{22})(1+s_{11}) - s_{12}\, s_{21}}\right] \frac{1}{Z_o}$$

Where Z_o = the characteristic impedance of the transmission lines used in the scattering parameter system, usually 50 ohms.

Conversion between h parameters and s parameters:

$$s_{11} = \frac{(h_{11}-1)(h_{22}+1) - h_{12}\, h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\, h_{21}} \dagger\dagger$$

$$s_{12} = \frac{2h_{12}}{(h_{11}+1)(h_{22}+1) - b_{12}\, h_{21}} \dagger\dagger$$

$$s_{21} = \frac{-2h_{21}}{(h_{11}+1)(h_{22}+1) - b_{12}\, h_{21}} \dagger\dagger$$

$$s_{22} = \frac{(1+h_{11})(1-h_{22}) + h_{12}\, h_{21}}{(h_{11}+1)(h_{22}+1) - h_{12}\, h_{21}} \dagger\dagger$$

$$b_{11} = \left[\frac{(1+s_{11})(1+s_{22}) - s_{12}\, s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\, s_{21}}\right] Z_o$$

$$h_{12} = \frac{2s_{12}}{(1-s_{11})(1+s_{22}) + s_{12}\, s_{21}}$$

$$h_{21} = \frac{-2s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\, s_{21}}$$

$$h_{22} = \left[\frac{(1-s_{22})(1-s_{11}) - s_{12}\, s_{21}}{(1-s_{11})(1+s_{22}) + s_{12}\, s_{21}}\right] \frac{1}{Z_o}$$

---

† In converting from y to s parameters, the y parameters must first be multiplied by Z_o and then substituted in the equations for conversion to s parameters.

†† In converting from h to s parameters, the h parameters must first be normalized to Z_o in the following manner and then substituted in the equations for conversion to s parameters:

Parameter	To Normalize
h_{11}	divide by Z_o
h_{12}	use as is
h_{21}	use as is
h_{22}	multiply by Z_o

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